15.6'' Grant 1.0 / 17.3'' Bogart 1.0

Intel Huron River Sandy Bridge 32nm SV PGA988B i3, i5 DC 35W/ i7 QC 45W

15.6'',17.3'' GDDR5 x 4(1GB), Seymour XT M2(29x29) 15W Muxless Hybrid Switchable
15.6'',17.3'' GDDR5 x8(1GB,2GB), Whistler XT M2(29x29) 35W Muxless Hybrid Switchable

POWER

- Adapter-in Jack w/Smart pin
- DC in Conn
- Battery Conn
- CHARGER: +VCHGR — 40
- 3.3VSTBY / 5VSTBY — 41
- DDR3: 1.5V / 0.75VS_DDR_VTT
- DDR_VTTR — 46
- CPU CORE
- 45W/35W : CPU_CORE — 42, 43
- CPU PLL : 1.8VS LDO — 47
- 1.1V LDO : USB3.0 — 37
- UMA in CPU: VGFX_CORE — 43
- CPU IO: 1.05VS_VCCIO
- == PCH CORE: 1.05VS — 44
- CPU IO(0.9V~0.8V): VCCSA — 45
- POWER GOOD — 38
- RUN POWER /SUS POWER — 39
- POWER GOOD — 39
- 5VSTBY ---> 5VS — 39
- 1.5V ---> 1.5VS == 1.5VS_CPUVDDQ — 39
- 3.3VSTBY---> 3.3VS — 39
- 3.3VSTBY---> 3.3VSTBY_PCH — 39
- 3.3VSTBY---> 3.3V_LAN — 39

POWER of Discrete VGA

- VGA_CORE — 57
- 35W /25W / 15W: VGA_CORE
- LDO: VGA_1.0VS — 56
- LDO: VGA_1.8VS — 56
- 3.3VS == VGA_3.3VS — 56
- 1.5V ---> VGA_1.5VS — 56
- BACO — 56
- DGPU_PWROK — 56
- DGPU_PERST#

Intel CPU

Sandy Bridge
Socket 989

2Phase35W
PEG 16Lanes

3Phase45W: support Turbo mode

DDR3 Dual Channel

2~8

Integrated Graphic Controller

DP

XDP

PEG x8

DMI

FDI

DDR3
1333/ 1600 someQC

- 9 DDR3-SODIMM
- 10 DDR3-SODIMM

27MHz X'TAL

27/100MHz CLK GEN

GPU AMD — 48~53

15.6''/17.3'' Muxless Hybrid:
Whistler XT 128bit 35W + gDDR5 x8
M2 package 29 x 29 FCBGA962

CH A
CH B

15.6''/17.3''
1GB/2GB Frame Buffer — 54~55
64Mx16 x8/128Mx16 x8
GDDR5, 5Gbps,12 x14mm

SPI ROM 128KB — SPI

DP → 4Lanes → eDP Panel Conn (4 Lanes conn)
Intel HR: Factory Option

Platform Control Hub

Intel PCH Cougar Point M
HM65 Express Chipset

Cougar Point M
Standard package
not SFF
3.9Watt TDP
FCBGA989
25mm X 25mm

12~21

X'TAL 14.318MHz
X'TAL 25MHz

HDMI 1.4 — 4Lanes — Base Line — HDMI Conn 24

RGB — Base Line — VGA Conn 22

LVDS — 1 ch 15" / 2 Ch 17" — Base Line — LVDS 23 (2 Channel Conn + USB 2.0)
USB 2.0: 480MBps — USB 2.0 — Cable
Touch Screen — Touch Screen: Factory Option
LVDS
17": 2 ch HD+ 1600x900
15" /15" Touch: 1 Ch HD 1366x768

USB 2.0: 480MBps
USB3.0 Factory Option

PCI-E Gen2 5GT/S — USB3.0 NEC uDP720200 36 — SuperSpeed USB 3.0 x2
- USB2.0/3.0 cnn Wake Up — Connecter co-layout 37
- USB2.0/3.0 cnn Wake Up — Connecter co-layout 37

Intel HR: add TUSB7320
AMD Sabine: no TUSB7320, Hudson-M3 for USB3.0
AMD Danube: add TUSB7320

PCI-E Gen2 5GT/S — Cardreader RTS5209 30 — Conn 30 — Cable — Conn
2 in 1 Slot: 1) SD/SDHC/SDXC UHS-104MByte/s, 208MHz 2) MMC 30

17.3'': daughter Board

30

USB 2.0: 480MBps — Conn 31 — Cable — Conn
- USB 2.0 Conn Wake Up
- USB 2.0 Conn Wake Up
- Standby LED — White: PWRon, White blink: S3
- HDD LED — Bi LEDx1, White: Normal , Amber: Park

15.6''/17.3'' daughter board

HDA

AUDIO CODEC IDT 92HD80TA — 33

- LDO TPS793475DBVR — 33
- SPK AMP TPA2012 — 34
  - Internal Speaker Conn x4 speakers
  - Internal DMic Conn To Webcam — 33, 34
  - Microphone x1 — 33
- HP AMP TPA6130A2 — 34
  - Headphone Microphone Combo Conn x2
- Woofer AMP TPA3111D1 — 35
  - WOOFER CONN — 35

34

for 17.3'' only

Lid Switch

LPC

KBC ITE8518 — 29

15.6'' daughter board

Conn — PWR Button x1 / White LEDx1 — White: PWR on, Blink White: Standby
Quick Web Button x1

17.3'' daughter board

Conn — PWR Button x1 / White LEDx1 — White: PWR on, Blink White: Standby
Quick Web Button x1

PWR D/B Conn 31 — Cable

T/P Pick Button board — 27

- T/P Pick Button — 15.6''/17.3'' daughter board
- Touch Pad Side Light LED Module — Touch Pad Side Light LED Module White x 4, T/P on/off LED Amber x1
- Touchpad Conn 27 — T/P Off: tapping T/P left-Top corner

Keyboard Conn 29 — KB with: White LEDx1: Cap lock, Amber LEDx1:Mute, White/Amber Bi LEDx1: wireless, NumLock LED x1: 15/17numberpad KB

Keyboard Backlight cnn 27 — Configureable

Thermal — Remote GPU Local CPU 27

FAN Conn 27 — Cable embeded

HP Logo LED Module Conn — Cable embeded White LED x 1

Charge LED — 40 — on Adaptor Jack, Bi LED x1, White: AC in, Amber: Charging

G SENSOR 25 — ST Micro HP3DC

SPI ROM BIOS 4MB — SPI

SPI ROM 512KB

RTC Cell Holder

X'TAL 32.768KHz

RTC

Realtek Gb LAN 30

RTL8111E-VB-GR
RTL8111E-VL-CG
W/ASPM
No cable pluged, the NIC auto disabled.

Transformer 30

RJ45 Jack 30 — LED White x1 for connectivity, Amber x1 for activity

WLAN/ WLAN+WiMAX /WLAN+BT 27

Half Size MiniCard Socket

PCI-E Gen2 5GT/S

USB 2.0

- Bluetooth Conn — Softbreeze Module 26 — EMBD BT2.1 SB FW299.306 ENH DTA RATE A
- WebCam Conn — Sensor OVT 9726 26 — Dual DMic, White LED: Enable
- Fingerprint Conn — Validaty VFM5131 26 — Bi LED x1: White normal, Amber not reconized

Cable

for 17.3'' only

- HDD Conn 2nd 25 — Cable
- HDD Conn 25 — Cable — SATA 3: 6Gbps
- ODD Conn 25 — Zero Power ODD Intel: Saving 100 ~ 160mW — Cable — SATA 2: 3Gbps

USB 2.0: 480MBps

Layout
DMI
Differential 85ohm (single 50)
n,p mismatch <5mils
maximum mis-match between inter-pairs : 7000 mils (177.8 mm)
Max: [2000 to 8000 mils, 3vias]
436735 Huron River Design Guide 1.0

Layout
FDI
Differential 85ohm (single 50)
n,p mismatch <5mils
pair to pair mismatch < 7 inches
Max:
3vias : 2000 to 8000 mils
4vias : 2000 to 6500 mils
436735 Huron River Design Guide 1.0

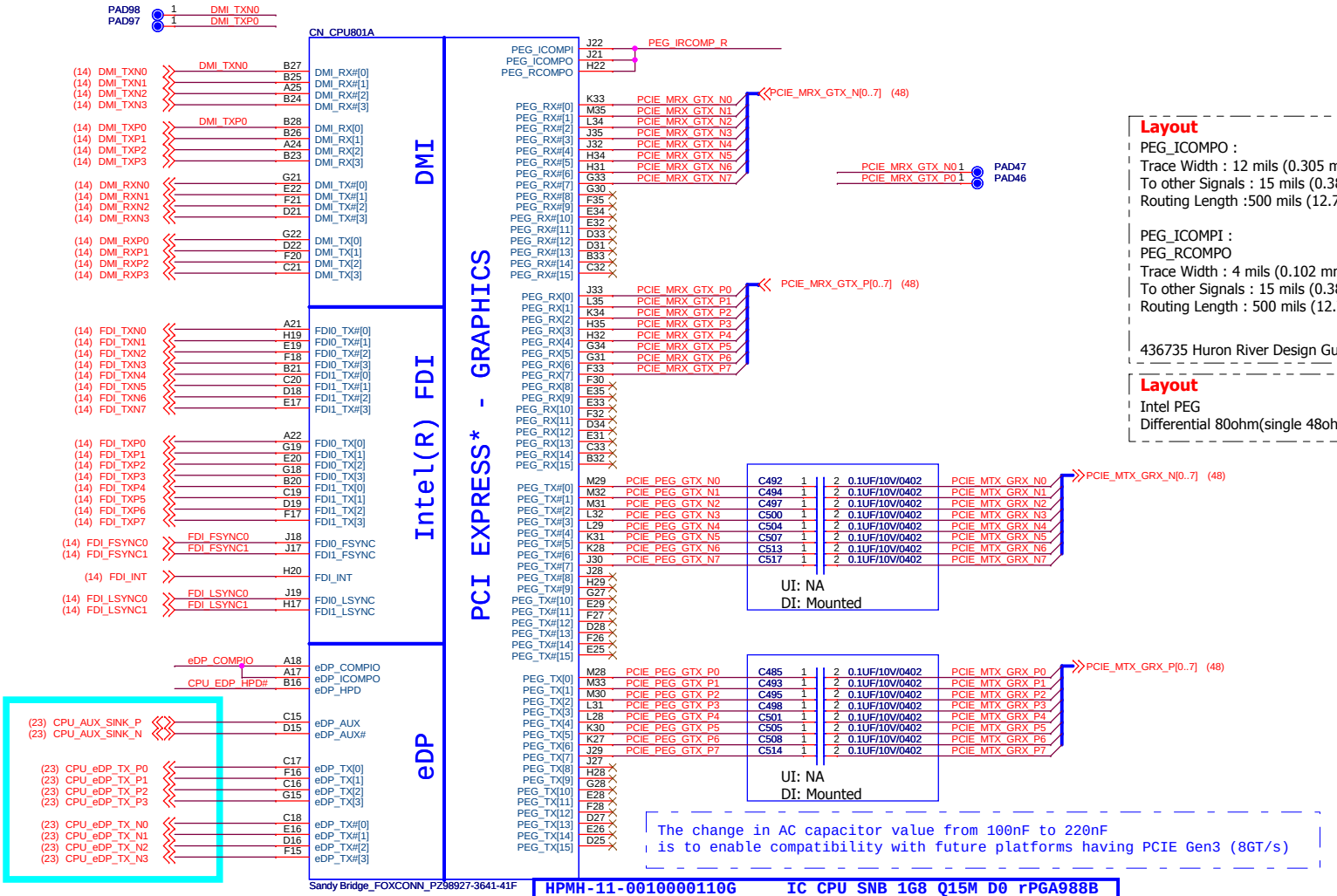
Note:
FDI (Flexible Display Interface):
Carries display traffic
from the integrated graphics controller
to the legacy display connectors in the PCH.

Layout
DP_ICOMPO :
Trace Width : 12 mils (0.305 mm)
To other Signals : 15 mils (0.381 mm)
Routing Length :500 mils (12.7 mm)

DP_COMPIO :
PEG_RCOMPO
Trace Width : 4 mils (0.102 mm)
To other Signals : 15 mils (0.381 mm)
Routing Length : 500 mils (12.7 mm)
436735 Huron River Design Guide 1.0

Layout
eDP
Differential 85ohm (single 50)
n,p mismatch <5mils
pair to pair mismatch < 7 inches
Max:
2vias : 2000 - 8000 mils
4vias : 2000 - 8000 mils
436735 Huron River Design Guide 1.0

Layout(Switchable Graphics Topology)
eDP
Differential 85ohm (single 50)
n,p mismatch <5mils
pair to pair mismatch < 7 inches
Max:
4vias : 2000 - 5000 mils
436735 Huron River Design Guide 1.0



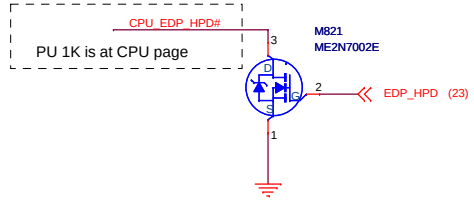
Layout
PEG_ICOMPO :
Trace Width : 12 mils (0.305 mm)
To other Signals : 15 mils (0.381 mm)
Routing Length :500 mils (12.7 mm)

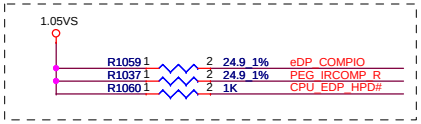
PEG_ICOMPI :
PEG_RCOMPO
Trace Width : 4 mils (0.102 mm)
To other Signals : 15 mils (0.381 mm)
Routing Length : 500 mils (12.7 mm)

436735 Huron River Design Guide 1.0

Layout
Intel PEG
Differential 80ohm(single 48ohm)

The change in AC capacitor value from 100nF to 220nF
is to enable compatibility with future platforms having PCIE Gen3 (8GT/s)

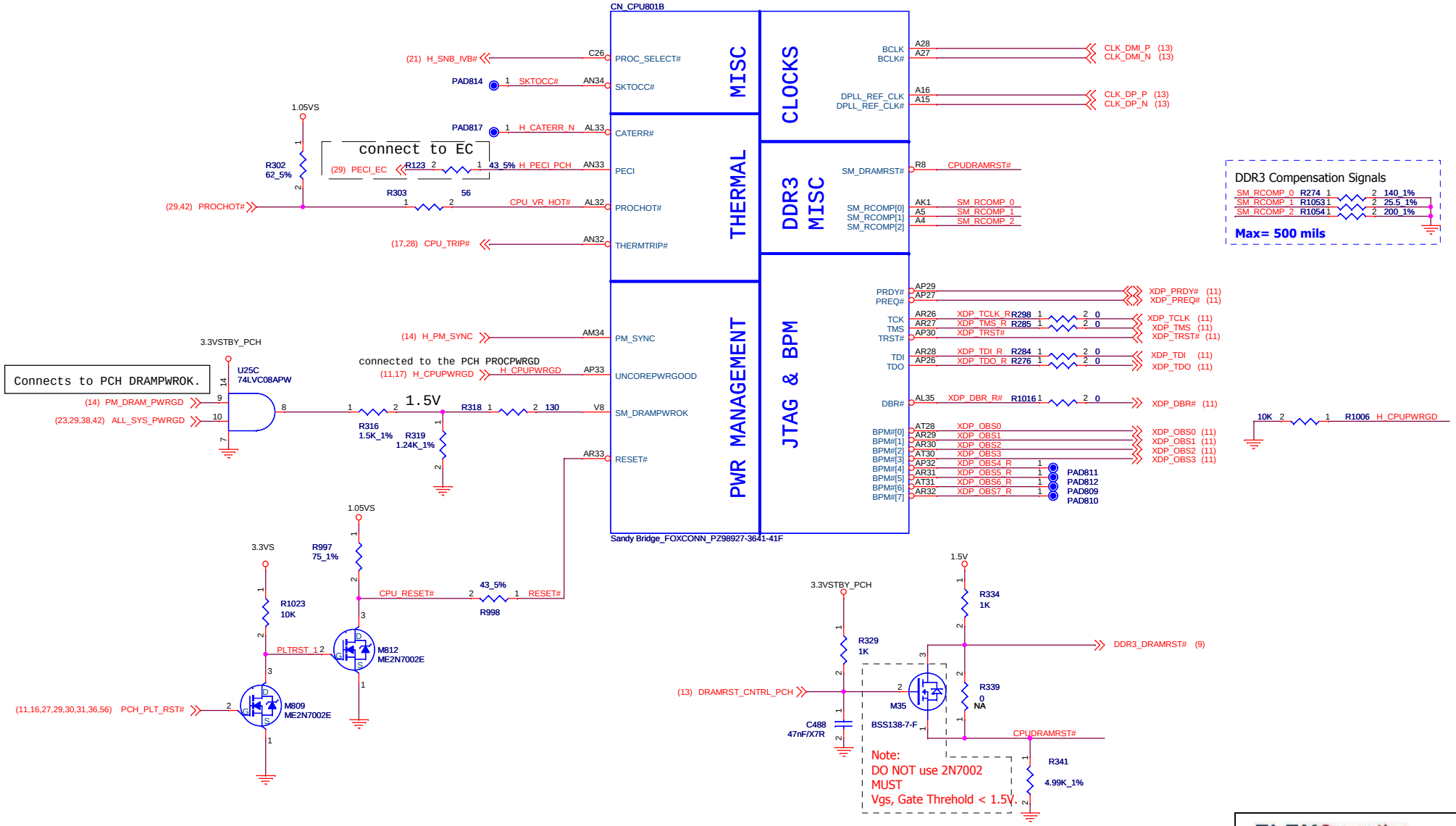


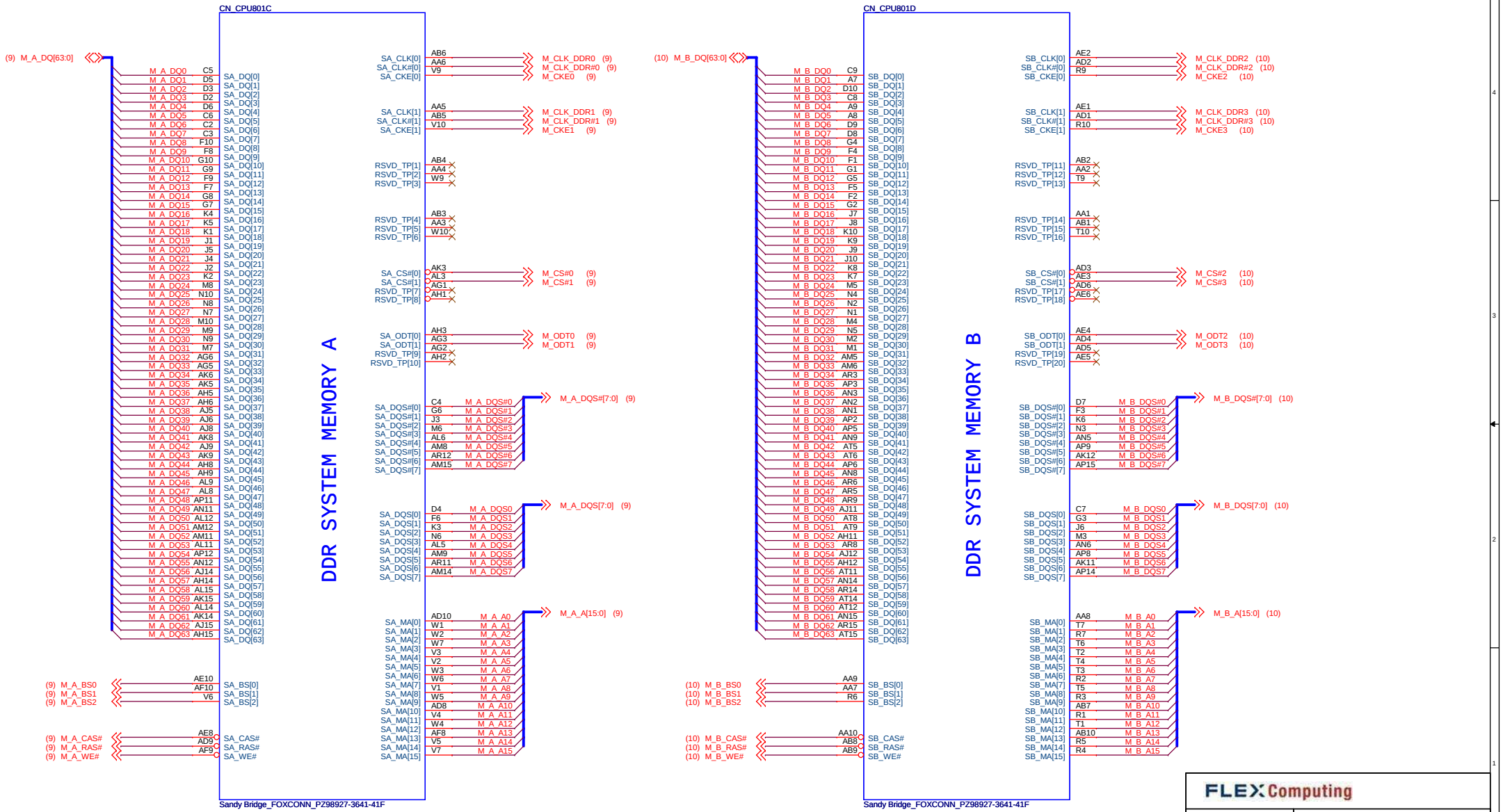


HPMH-11-0010000110G	IC CPU SNB 1G8 Q15M D0 rPGA988B
HPMH-11-0010000111G	IC CPU SNB 2G Q15C D0 rPGA988B
HPMH-11-0010000112G	IC CPU SNB 2G2 Q154 D0 rPGA988B
HPMH-11-0010000113G	IC CPU SNB 2G5 Q17N J0 rPGA988B
HPMH-11-0010000114G	IC CPU SNB 2G6 Q16P J0 rPGA988B
HPMH-11-0010000115G	IC CPU SNB 2G7 Q16M J0 rPGA988B
HPMH-11-0010000116G	IC CPU SNB 2G5 Q17N J0 rPGA988B
HPMH-11-0010000117G	IC CPU SNB 2G2 Q1CL D1 rPGA988B
HPMH-11-0010000118G	IC CPU SNB 2G3 Q1CG D1 rPGA988B
HPMH-11-0010000119G	IC CPU SNB 2G Q1CN D1 rPGA988B
HPMH-11-0010000120G	IC CPU SNB 2G Q1NS D2 rPGA988B
HPMH-11-0010000121G	IC CPU SNB 2G2 Q1NN D2 rPGA988B
HPMH-11-0010000122G	IC CPU SNB 2G3 Q1NC D2 rPGA988B
HPMH-11-0010000123G	IC CPU SNB 2G1 Q1SP J1 rPGA988B
HPMH-11-0010000124G	IC CPU SNB 2G3 Q1SD J1 rPGA988B
HPMH-11-0010000125G	IC CPU SNB 2G5 Q1RX J1 rPGA988B
HPMH-11-0010000126G	IC CPU SNB 2G6 Q1S6 J1 rPGA988B
HPMH-11-0010000127G	IC CPU SNB 2G7 Q1S2 J1 rPGA988B
HPMH-11-0010000128G	IC CPU SNB 2G SR02Y D2 rPGA988B
HPMH-11-0010000129G	IC CPU SNB 2G2 SR014 D2 rPGA988B
HPMH-11-0010000130G	IC CPU SNB 2G3 SR012 D2 rPGA988B

FLEX Computing

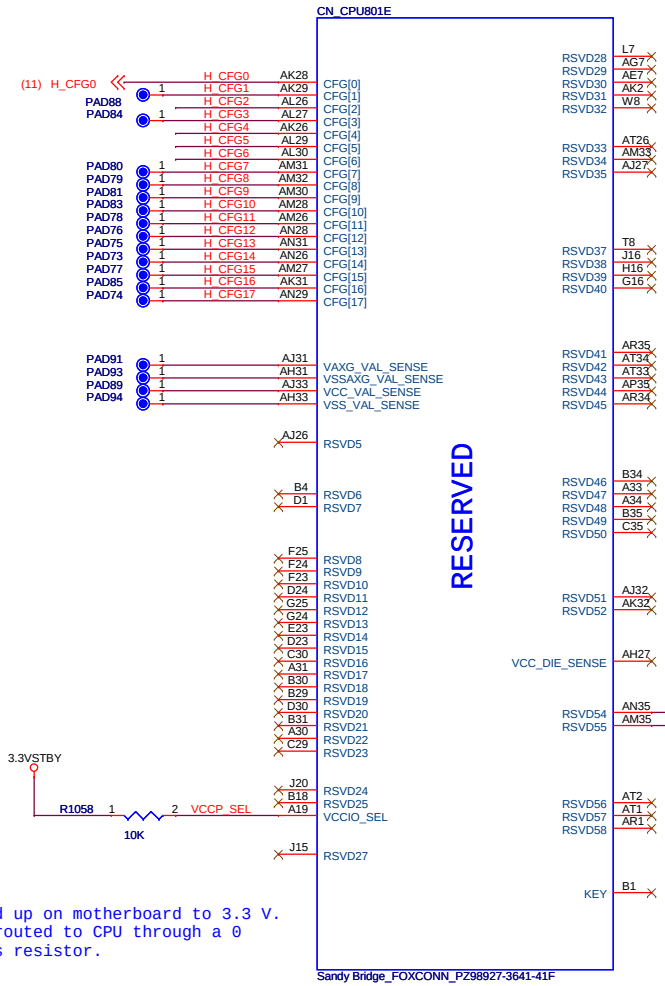
Project Name : H710DI1	Title : CPU_1/7_DMI_FDI_PCIE	
Size :	Document Number : HPMH-40GAB6600-B130	Rev : B
Date: Monday, November 08, 2010	Sheet : 2 of 63	


CN_CPU801B
MISC
CLOCKS
THERMAL
DDR3 MISC
PWR MANAGEMENT
JTAG & BPM
PROC_SELECT#
SKTOCC#
CATERR#
PECI
PROCHOT#
THERMTRIP#
PM_SYNC
UNCOREPWRGOOD
SM_DRAMPWROK
RESET#
BCLK
BCLK#
DPLL_REF_CLK
DPLL_REF_CLK#
SM_DRAMRST#
SM_RCOMP[0]
SM_RCOMP[1]
SM_RCOMP[2]
PRDY#
PREQ#
TCK
TMS
TRST#
TDI
TDO
DBR#
BPM#[0]
BPM#[1]
BPM#[2]
BPM#[3]
BPM#[4]
BPM#[5]
BPM#[6]
BPM#[7]
Sandy Bridge_FOXCONN_PZ98927-3641-41F
connect to EC
connected to the PCH PROCPWRGD
Connects to PCH DRAMPWROK.
DDR3 Compensation Signals
Max= 500 mils
Note:
DO NOT use 2N7002
MUST
Vgs, Gate Threhold < 1.5V.
FLEX Computing
Project Name : H710DI1
Title : CPU_2/7_CLK_MISC_THERM
Size :
Document Number : HPMH-40GAB6600-B130
Rev : B
Date: Monday, November 08, 2010
Sheet : 3 of 63



FLEX Computing

Project Name : H710DI1	Title : CPU_3/7_DDR3	
Size :	Document Number : HPMH-40GAB6600-B130	Rev : B
Date: Monday, November 08, 2010	Sheet : 4 of 63	



Pulled up on motherboard to 3.3 V.
Also routed to CPU through a 0 series resistor.

VCCIO_SEL On CRB
H_SNB_IVB#_PWRCTRL = low, 1.0V
H_SNB_IVB#_PWRCTRL = high/NC, 1.05V

Voltage selection for VCCIO: For Huron River platforms, this pin must be pulled high on the motherboard

Sandy Bridge_FOXCONN_PZ98927-3641-41F

CFG Straps for PROCESSOR

H_CFG5 H_CFG6 — R267 1 2 1K — PAD82

PCIE Port Bifurcation Straps

CFG[6:5]	11:(Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled function 2 disabled 01: Reserved - Device 1 function 1 disabled function 2 enabled 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

H_CFG7 — R258 1 2 1K NA

PEG DEFER TRAINING

CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

CFG[17:7]	Reserved configuration lanes. A test point may be placed on the board for these lands.

CFG[1:0]	Reserved configuration lane. A test point may be placed on the board for this lane.

H_CFG2 — 1 — PAD86

PEG Static Lane Reversal - CFG2 is for the 16x

CFG[2]	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane numbers reversed

H_CFG3 — 1 — PAD87

PCI Express* Static x4 Lane Numbering Reversal.

CFG[3]	1 : Normal operation 0 : Lane numbers reversed

H_CFG4 — R269 1 2 1K — NA

LVDS NA eDP Mount

Display Port Presence Strap(eDP enable)

CFG[4]	1:(Default) Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

FLEX Computing

Project Name : H710DI1	Title : CPU_4/7_RSVD_CFG	
Size :	Document Number : HPMH-40GAB6600-B130	Rev : B
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POWER

CN_CPU801F

PEG AND DDR

CORE SUPPLY

36A~52A

CPU_CORE

C1055 10UF/6.3V/0603
C459 10UF/6.3V/0603
C1062 10UF/6.3V/0603
C412 10UF/6.3V/0603
C460 10UF/6.3V/0603
C457 10UF/6.3V/0603
C461 10UF/6.3V/0603
C458 10UF/6.3V/0603
C436 10UF/6.3V/0603
C435 10UF/6.3V/0603
C1059 22UF/6.3V/0805
C1056 22UF/6.3V/0805
C416 22UF/6.3V/0805
C438 22UF/6.3V/0805
C437 22UF/6.3V/0805
C1057 22UF/6.3V/0805
C1058 22UF/6.3V/0805
C1063 22UF/6.3V/0805
C1065 22UF/6.3V/0805
C413 22UF/6.3V/0805
C414 22UF/6.3V/0805
C439 22UF/6.3V/0805
C440 22UF/6.3V/0805
C1066 22UF/6.3V/0805
C415 22UF/6.3V/0805
C408 330UF/2.5V/1.9mm
C487 330UF/2.5V/1.9mm
C1064 22UF/6.3V/0805
modify for FN

AG35 VCC1
AG34 VCC2
AG33 VCC3
AG32 VCC4
AG31 VCC5
AG30 VCC6
AG29 VCC7
AG28 VCC8
AG27 VCC9
AG26 VCC10
AF35 VCC11
AF34 VCC12
AF33 VCC13
AF32 VCC14
AF31 VCC15
AF30 VCC16
AF29 VCC17
AF28 VCC18
AF27 VCC19
AF26 VCC20
AD35 VCC21
AD34 VCC22
AD33 VCC23
AD32 VCC24
AD31 VCC25
AD30 VCC26
AD29 VCC27
AD28 VCC28
AD27 VCC29
AD26 VCC30
AC35 VCC31
AC34 VCC32
AC33 VCC33
AC32 VCC34
AC31 VCC35
AC30 VCC36
AC29 VCC37
AC28 VCC38
AC27 VCC39
AC26 VCC40
AA35 VCC41
AA34 VCC42
AA33 VCC43
AA32 VCC44
AA31 VCC45
AA30 VCC46
AA29 VCC47
AA28 VCC48
AA27 VCC49
AA26 VCC50
Y35 VCC51
Y34 VCC52
Y33 VCC53
Y32 VCC54
Y31 VCC55
Y30 VCC56
Y29 VCC57
Y28 VCC58
Y27 VCC59
Y26 VCC60
V35 VCC61
V34 VCC62
V33 VCC63
V32 VCC64
V31 VCC65
V30 VCC66
V29 VCC67
V28 VCC68
V27 VCC69
V26 VCC70
U35 VCC71
U34 VCC72
U33 VCC73
U32 VCC74
U31 VCC75
U30 VCC76
U29 VCC77
U28 VCC78
U27 VCC79
U26 VCC80
R35 VCC81
R34 VCC82
R33 VCC83
R32 VCC84
R31 VCC85
R30 VCC86
R29 VCC87
R28 VCC88
R27 VCC89
R26 VCC90
P35 VCC91
P34 VCC92
P33 VCC93
P32 VCC94
P31 VCC95
P30 VCC96
P29 VCC97
P28 VCC98
P27 VCC99
P26 VCC100

1.05VS

8.5A

MB Bottom Socket Cavity

C1061 22UF/6.3V/0805
C1069 22UF/6.3V/0805
C1071 22UF/6.3V/0805
C453 22UF/6.3V/0805
C469 22UF/6.3V/0805

MB Top Socket Cavity

C478 22UF/6.3V/0805
C1068 22UF/6.3V/0805
C1076 22UF/6.3V/0805
C1084 22UF/6.3V/0805
C1085 22UF/6.3V/0805
C523 22UF/6.3V/0805
C1082 22UF/6.3V/0805
C534 330UF/2.5V/1.9mm

VCCIO at CPU

AH13 VCCIO1
AH10 VCCIO2
AG10 VCCIO3
AC10 VCCIO4
Y10 VCCIO5
U10 VCCIO6
P10 VCCIO7
L10 VCCIO8
J14 VCCIO9
J13 VCCIO10
J12 VCCIO11
J11 VCCIO12
H14 VCCIO13
H12 VCCIO14
H11 VCCIO15
G14 VCCIO16
G13 VCCIO17
G12 VCCIO18
F14 VCCIO19
F13 VCCIO20
F12 VCCIO21
F11 VCCIO22
E14 VCCIO23
E12 VCCIO24
E11 VCCIO25
D14 VCCIO26
D13 VCCIO27
D12 VCCIO28
D11 VCCIO29
C14 VCCIO30
C13 VCCIO31
C12 VCCIO32
C11 VCCIO33
B14 VCCIO34
B12 VCCIO35
A14 VCCIO36
A13 VCCIO37
A12 VCCIO38
A11 VCCIO39
J23 VCCIO40

7/06 delet 330uF X2
poewr side have 330uF X3
(3x 330 µF for 2012 capable designs)
follow Huron River Platform Power Delivery (439028)

SVID

50 ohm reference GND

AJ29 VIDALERT# — SVID_ALRT_R# — R266 1 2 43_5% — VR_SVID_ALERT# (42)
AJ30 VIDSCLK — VR_SVID_CLK — VR_SVID_CLK (42)
AJ28 VIDSOUT — VR_SVID_DATA — VR_SVID_DATA (42)

1.05VS

VR_SVID_ALERT# R305 1 2 75_1%
VR_SVID_DATA R306 1 2 130_1%

Layout Note:
Alert#(AJ29) signal must be routed between the Clock and Data lines to reduce the cross talk between them. Spacing recommendations from the “Asynchronous Signal General Routing Guideline” of the Huron River PDG have to be met.

SENSE LINES

AJ35 VCC_SENSE — VCC_SENSE (42)
AJ34 VSS_SENSE — VSS_SENSE (42)

B10 VCCIO_SENSE — VCCIO_SENSE (44)
A10 VSSIO_SENSE — VSSIO_SENSE (44)

1.05VS

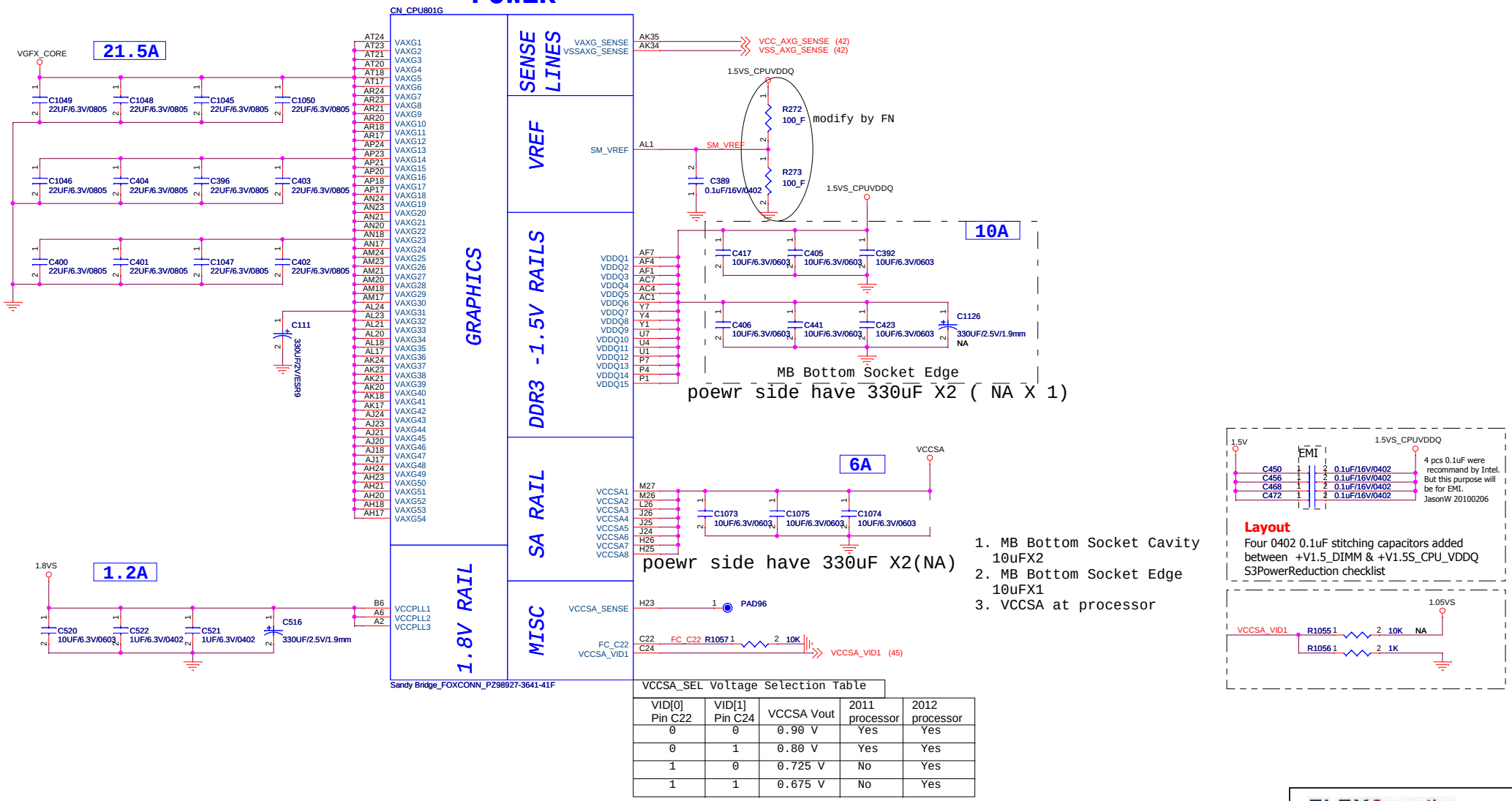
VCCIO_SENSE R343 1 2 10 NA
VSSIO_SENSE R345 1 2 10 NA

Sandy Bridge_FOXCONN_PZ98927-3641-41F

FLEX Computing

Project Name : H710DI1	Title : CPU_5/7_VCC_VCCIO
Size :	Document Number : HPMH-40GAB6600-B130 — Rev : B
Date: Monday, November 08, 2010	Sheet : 6 of 63

POWER



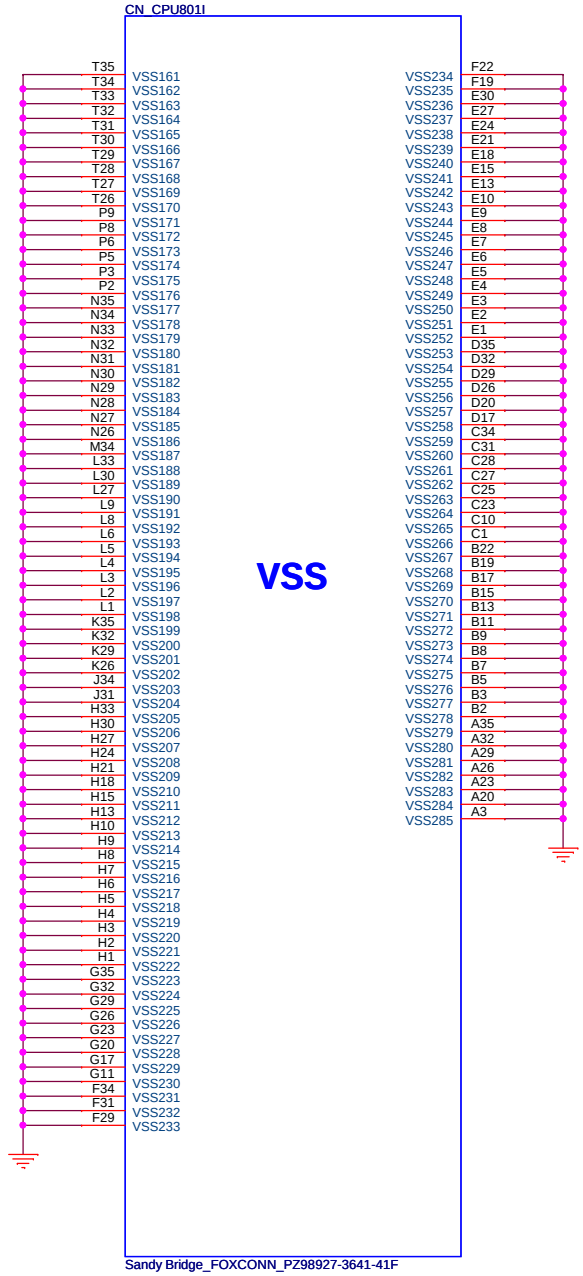
1. MB Bottom Socket Cavity 10uFX2
2. MB Bottom Socket Edge 10uFX1
3. VCCSA at processor

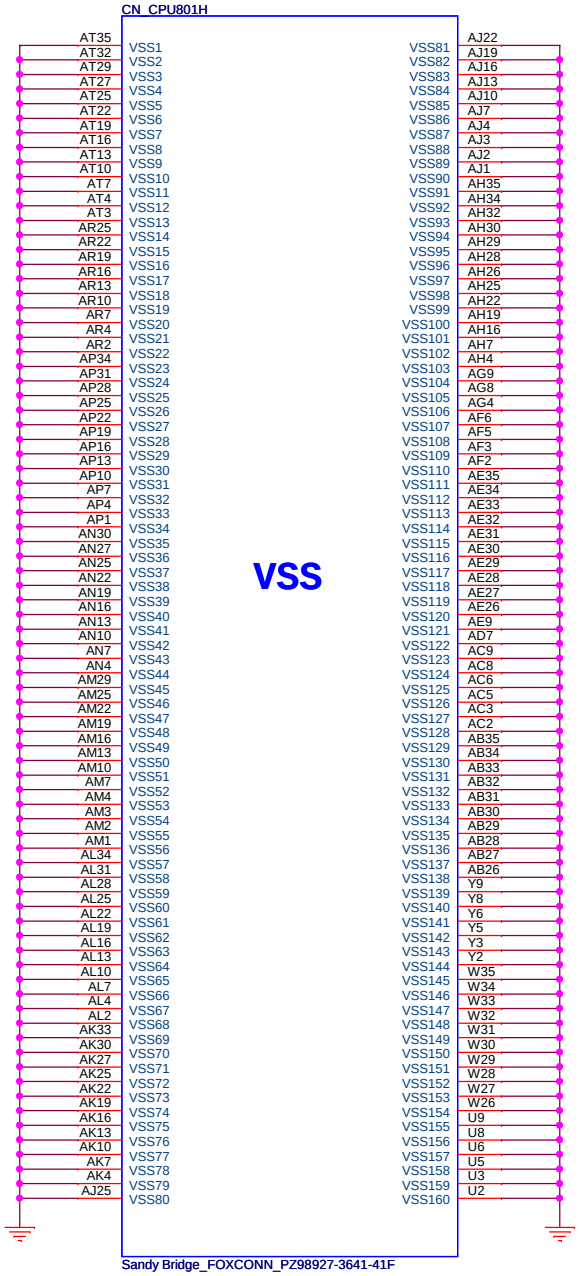
VCCSA_SEL Voltage Selection Table

VID[0] Pin C22	VID[1] Pin C24	VCCSA Vout	2011 processor	2012 processor
0	0	0.90 V	Yes	Yes
0	1	0.80 V	Yes	Yes
1	0	0.725 V	No	Yes
1	1	0.675 V	No	Yes

FLEX Computing

Project Name : H710DI1	Title : CPU_6/7_VGFX_VDDR3
Size :	Document Number : HPMH-40GAB6600-B130 Rev : B
Date: Monday, November 08, 2010	Sheet : 7 of 63

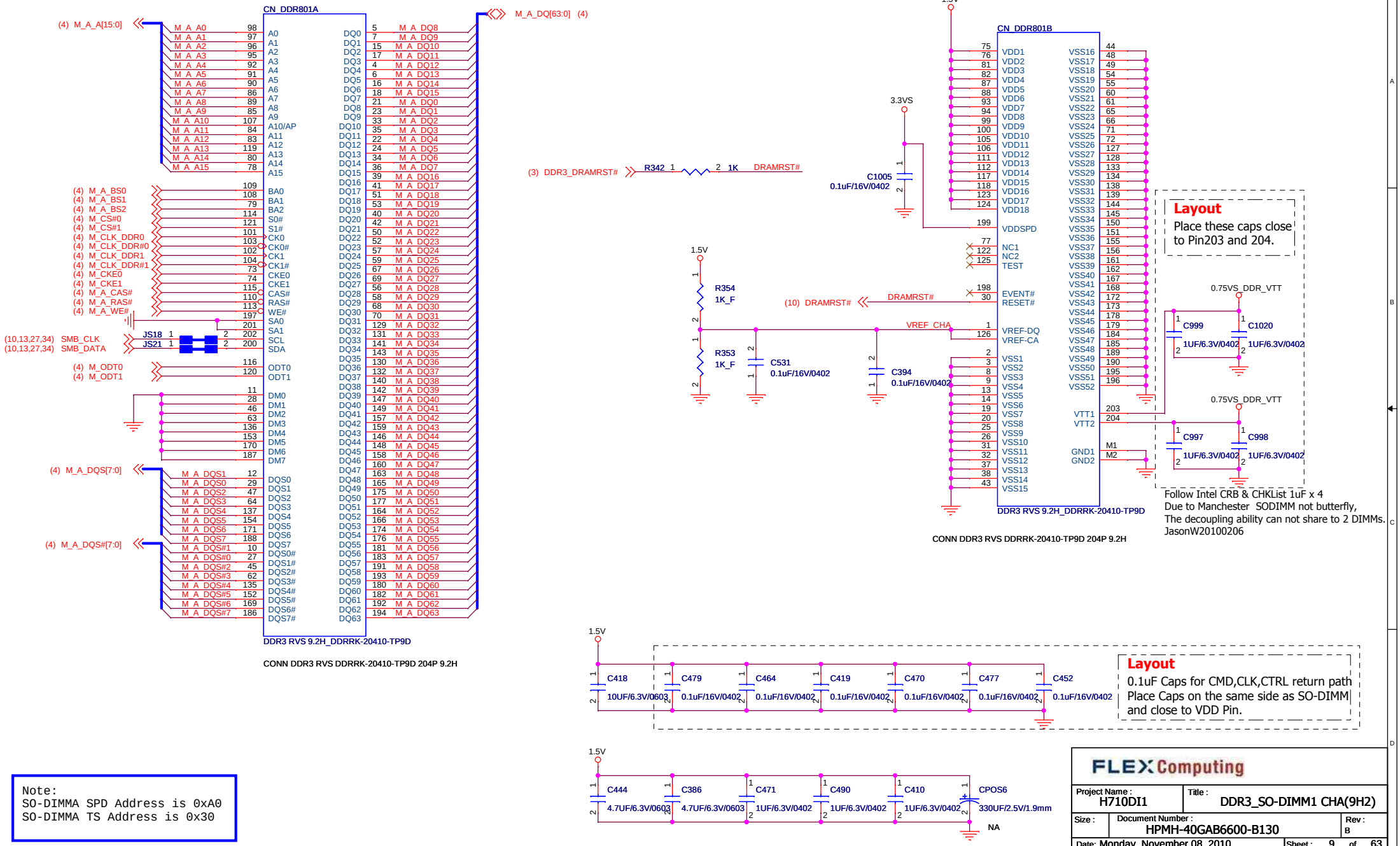




FLEXComputing

Project Name : H710DI1	Title : CPU_7/7_VSS	
Size :	Document Number : HPMH-40GAB6600-B130	Rev : B
Date: Monday, November 08, 2010	Sheet : 8 of 63	

Channel-A



Note:
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

FLEXComputing

Project Name : H710DI1	Title : DDR3_SO-DIMM1 CHA(9H2)
Size :	Document Number : HPMH-40GAB6600-B130 Rev : B
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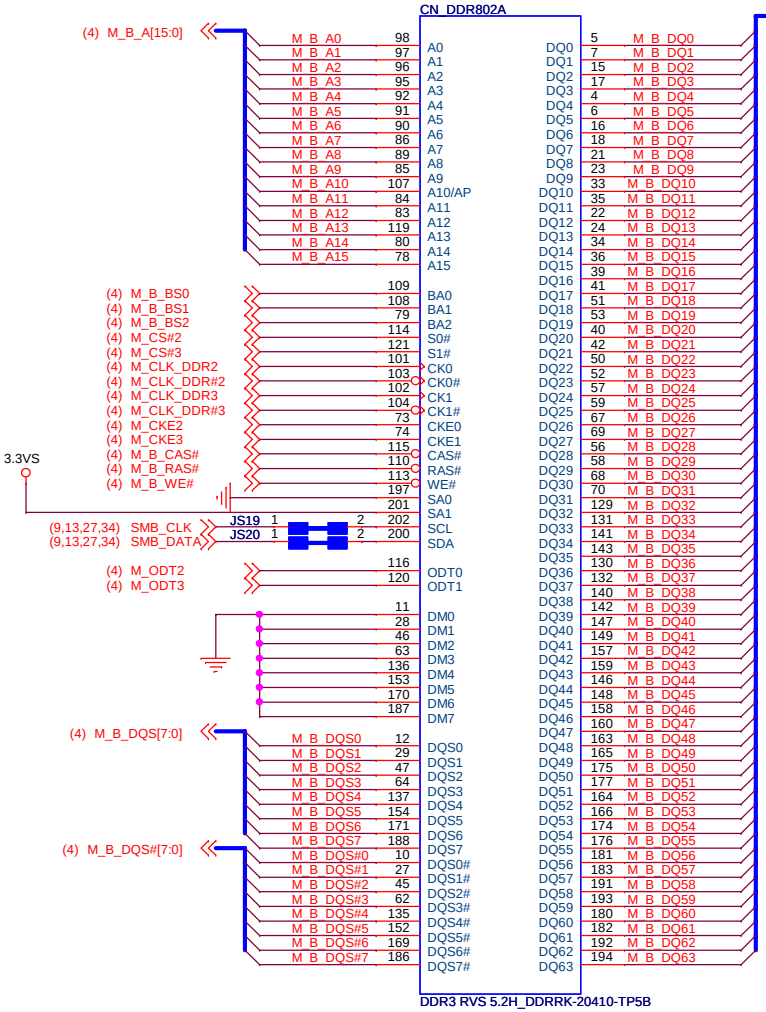
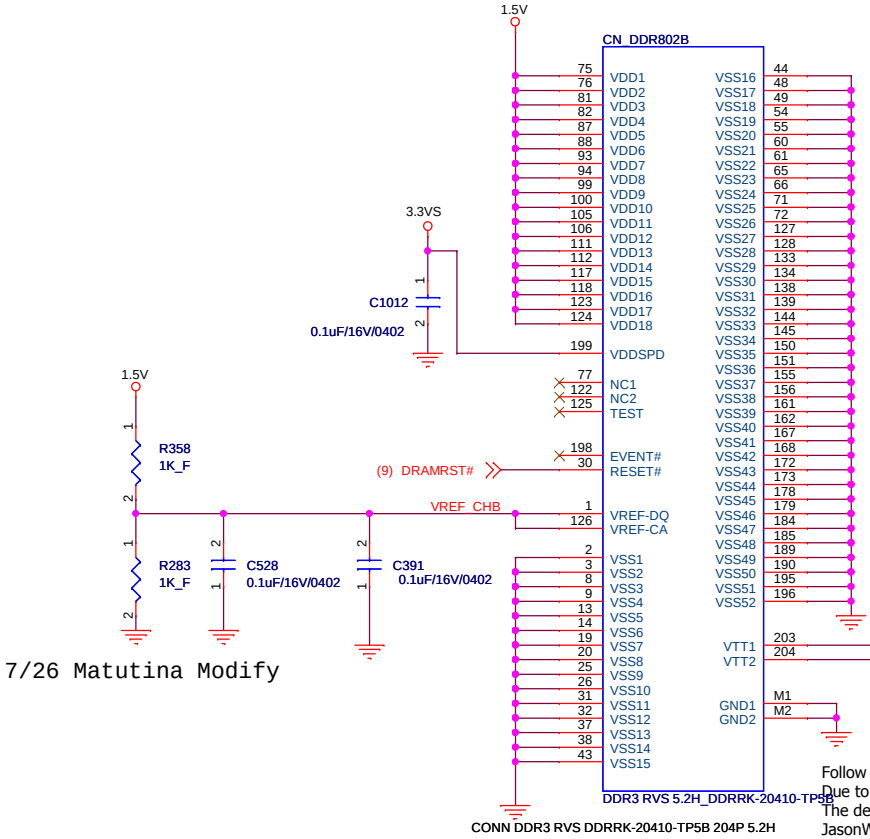
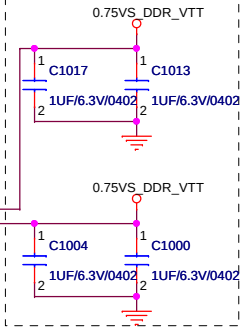
Channel-B

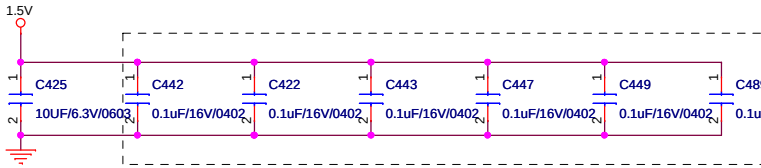




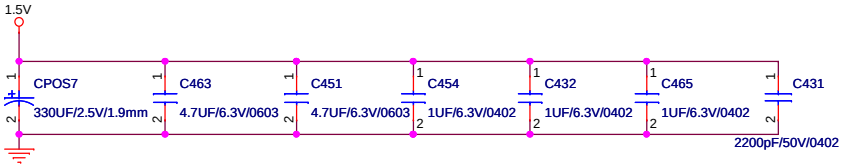
Layout
Place these caps close to Pin203 and 204.



Follow Intel CRB & CHKList 1uF x 4
Due to Manchester SODIMM not butterfly,
The decoupling ability can not share to 2 DIMMs.
JasonW20100206



Layout
0.1uF Caps for CMD,CLK,CTRL return path
Place Caps on the same side as SO-DIMM and close to VDD Pin .



Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMM Address		
SA0_DIM0 = 0, SA1_DIM0 = 0	SPD	0xA0
	TS	0x30
SA0_DIM1 = 0, SA1_DIM1 = 1	SPD	0xA4
	TS	0x34

FLEXComputing

Project Name : H710DI1	Title : DDR3_SO-DIMM2 CHB(5H2)
Size :	Document Number : HPMH-40GAB6600-B130 Rev : B
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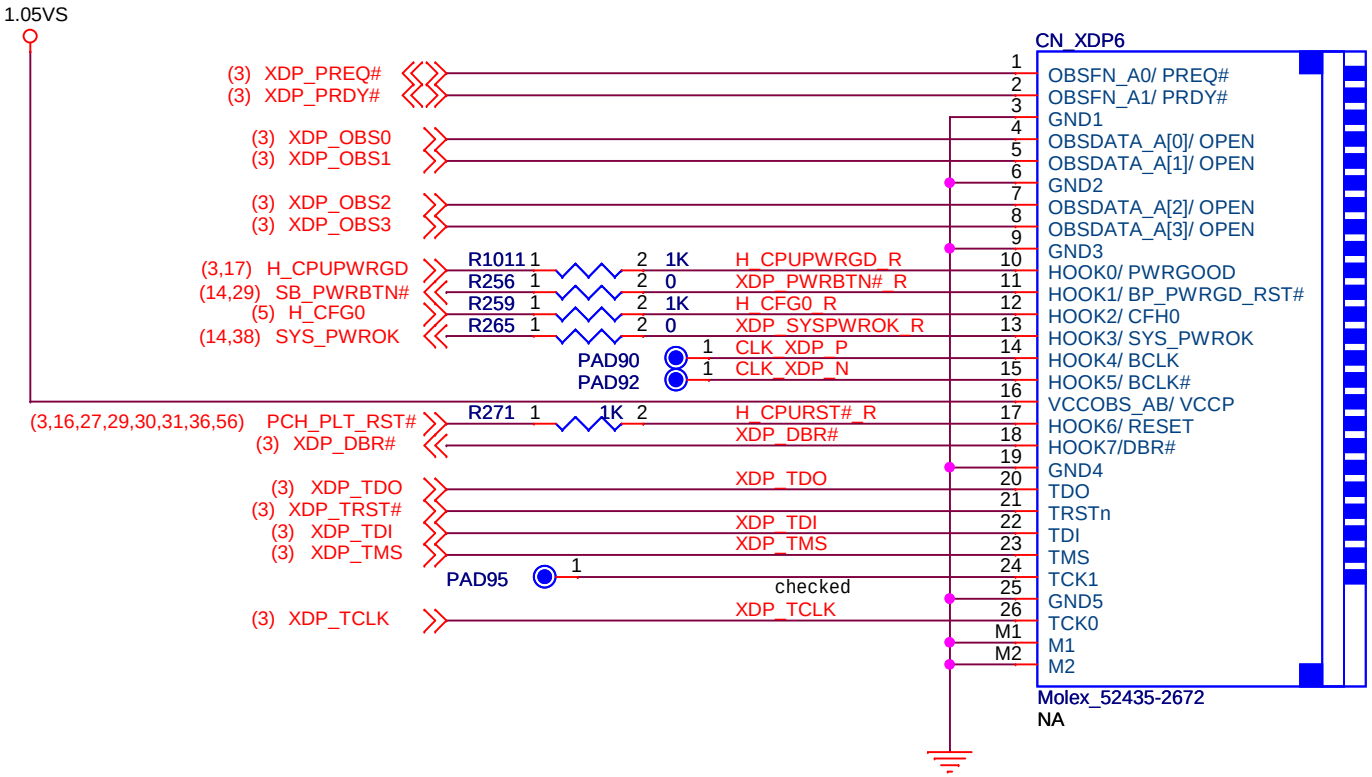
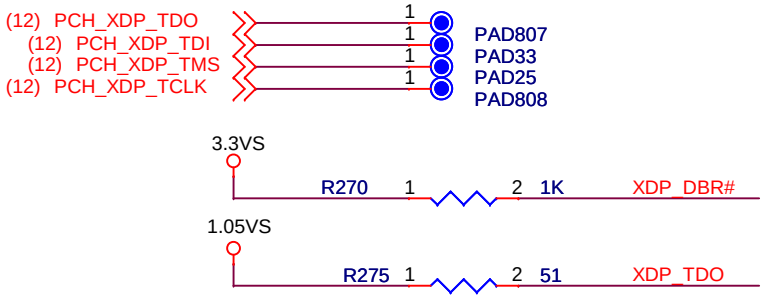
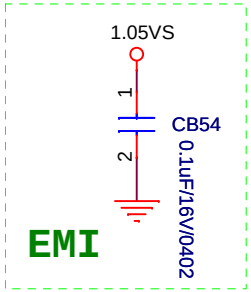
Debug Port







FLEX Computing

Project Name : H710DI1	Title : XDP(PROCESSOR / PCH)	
Size :	Document Number : HPMH-40GAB6600-B130	Rev : B
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COUGARPOINT (HDA,JTAG,SPI,SATA)

Internal Pull-Up and Pull-Down

	Mark
Pull-Up	P+
Pull-Down	P-

U811A

RTC: RTCX1, RTCX2, RTCRST#, SRTCRST#, INTRUDER#, INTVRMEN

LPC: FWH0 / LAD0, FWH1 / LAD1, FWH2 / LAD2, FWH3 / LAD3, FWH4 / LFRAME#, LDRQ0# / LDRQ1# / GPIO23, SERIRQ

IHDA: HDA_BCLK, HDA_SYNC, SPKR, HDA_RST#, HDA_SDIN0, HDA_SDIN1, HDA_SDIN2, HDA_SDIN3, HDA_SDO, HDA_DOCK_EN# / GPIO33, HDA_DOCK_RST# / GPIO13

JTAG: JTAG_TCK, JTAG_TMS, JTAG_TDI, JTAG_TDO

SPI: SPI_CLK, SPI_CS0#, SPI_CS1#, SPI_MOSI, SPI_MISO

SATA: SATA0RXN/P, SATA0TXN/P, SATA1RXN/P, SATA1TXN/P, SATA2RXN/P, SATA2TXN/P, SATA3RXN/P, SATA3TXN/P, SATA4RXN/P, SATA4TXN/P, SATA5RXN/P, SATA5TXN/P, SATAICOMPO, SATAICOMPI, SATA3RCOMPO, SATA3COMPI, SATA3RBIAS, SATALED#, SATA0GP / GPIO21, SATA1GP / GPIO19

CougarPoint_Rev_1p0

STRAP and Audio

STRAP

EMI

Close PCH

VTAP Assumed as 1.1V

17'' MOUNTED 15'' NA

15'' MOUNTED 17'' NA

Design Guide 1.2 (#436735)
HDA_SYNC Potential Leakage Concern

To HDD 1 for 15''

To HDD 2 for 17''

H61 SATA ports 2 and 3 are disabled

For BIOS power saving check

To ODD

TO INDICATE LED BOARD

HPMH-10-0010000113G	IC Cougar Point PCH QNDL FCBGA989(MH65)B1
HPMH-10-0010000115G	IC Cougar Point PCH QNJG FCBGA989(HM67)B2
HPMH-10-0010000116G	IC Cougar Point PCH QNJH FCBGA989(HM65)B2
HPMH-10-0010000117G	IC Cougar Point PCH SLH9D FCBGA989(HM65)B2

32Mbit (4M Byte) SPI

U814 EN25F32-100HIP HPMH-14-0090000064G

BIOS1 — BIOS Label — HPMH-B2685310G00016

HDMI0 — HDMI Label — HPMH-B2995007G00001

PCB1 — PCB — HPMH-41-AB6200-C00G

15'' RTC2 — RTC — BTRY LITHIUM COIN CR2032 JHT 3V 220mAh HPMH-83-2030000007G

17'' RTC3 — RTC_17inch — CABLE FOR RTC G AB650 HPMH-B3035050G00009 NA

FLEXComputing

Project Name : H710DI1	Title : PCH_1/10_LPC_ RTC_ HDA_SATA
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COUGARPOINT (PCI-E,SMBUS,CLK)

PCI-E 2.0 x1	Usage
Lane 1	LAN
Lane2	WLAN
Lane 3	Card Reader
Lane 4	USB3.0
Lane 5	
Lane 6	
Lane 7	
Lane 8	

LAN

WLAN

Card Reader

USB3.0

U811B

PCI-E*

SMBUS

Controller Link

CLOCKS

FLEX CLOCKS

For BIOS power saving check

7/19 Matutina Modify

TO Audio
TO SO-DIMM
TO WLAN

TO KBC

TO dGPU

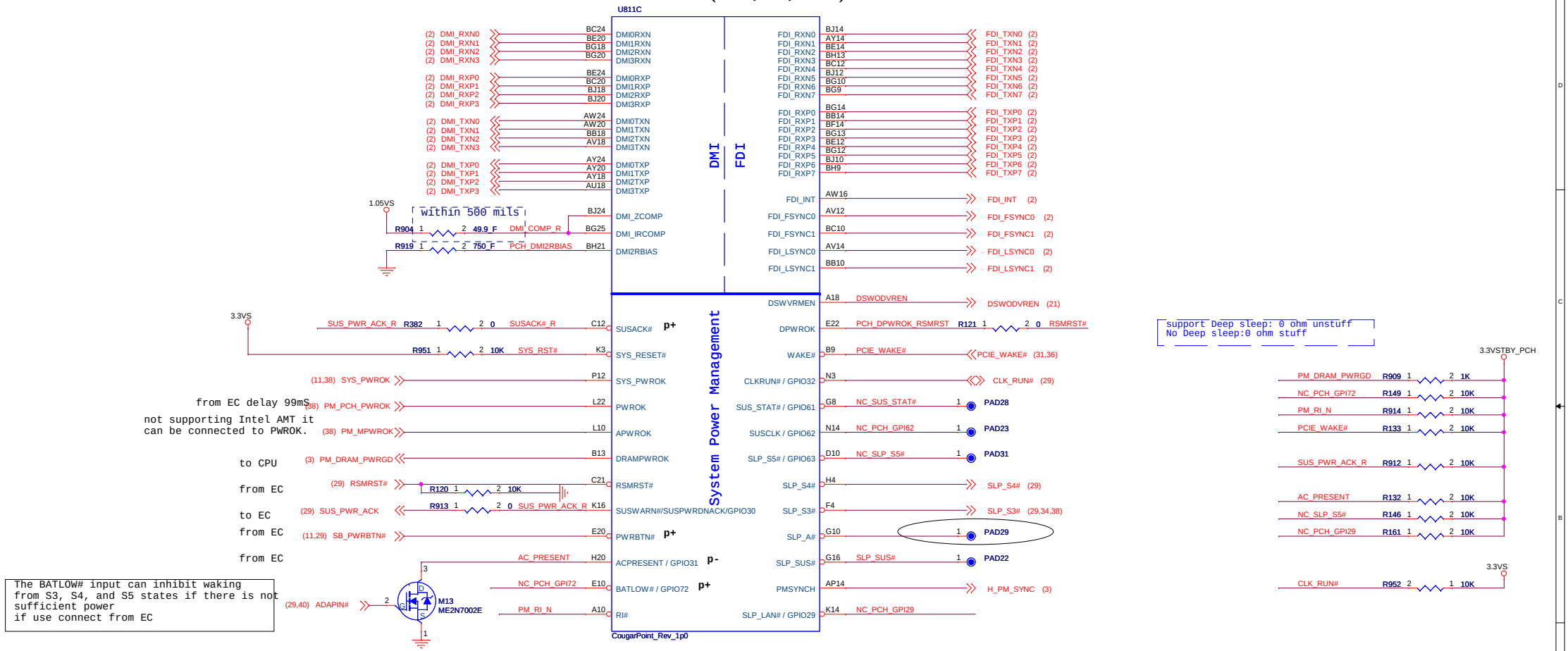
CRB use this pin to control DDR3_DRAMRST#

Clock termination for FCIM
1. External clock present: 10k unstuffed
2. External clock no present: 10k stuffed

EMI

CougarPoint_Rev_1p0

COUGARPOINT (DMI,FDI,GPIO)



FLEX Computing	
Project Name : H710DI1	Title : PCH_3/10_DMI_ FDI_SPM
Size :	Document Number : HPMH-40GAB6600-B130 Rev : B
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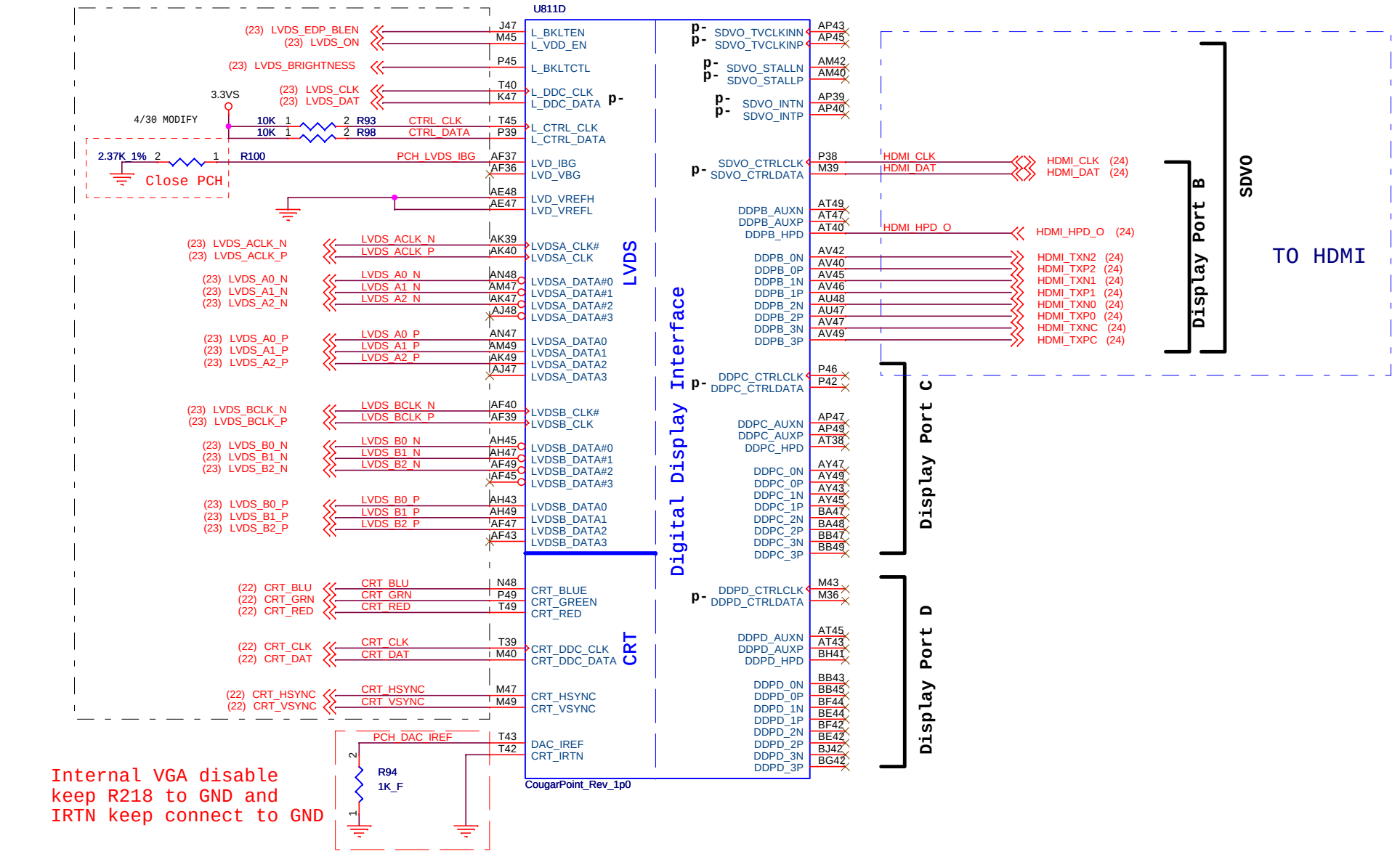
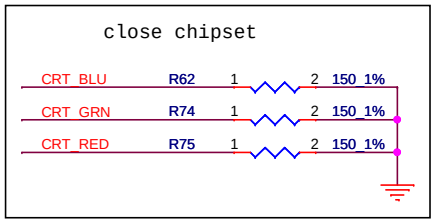
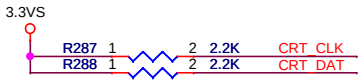
COUGARPOINT (LVDS,DDI)



close chipset





FLEX Computing

Project Name : H710DI1	Title : PCH_4/10_CRT_ LVDS_DDI
Size :	Document Number : HPMH-40GAB6600-B130 Rev : B
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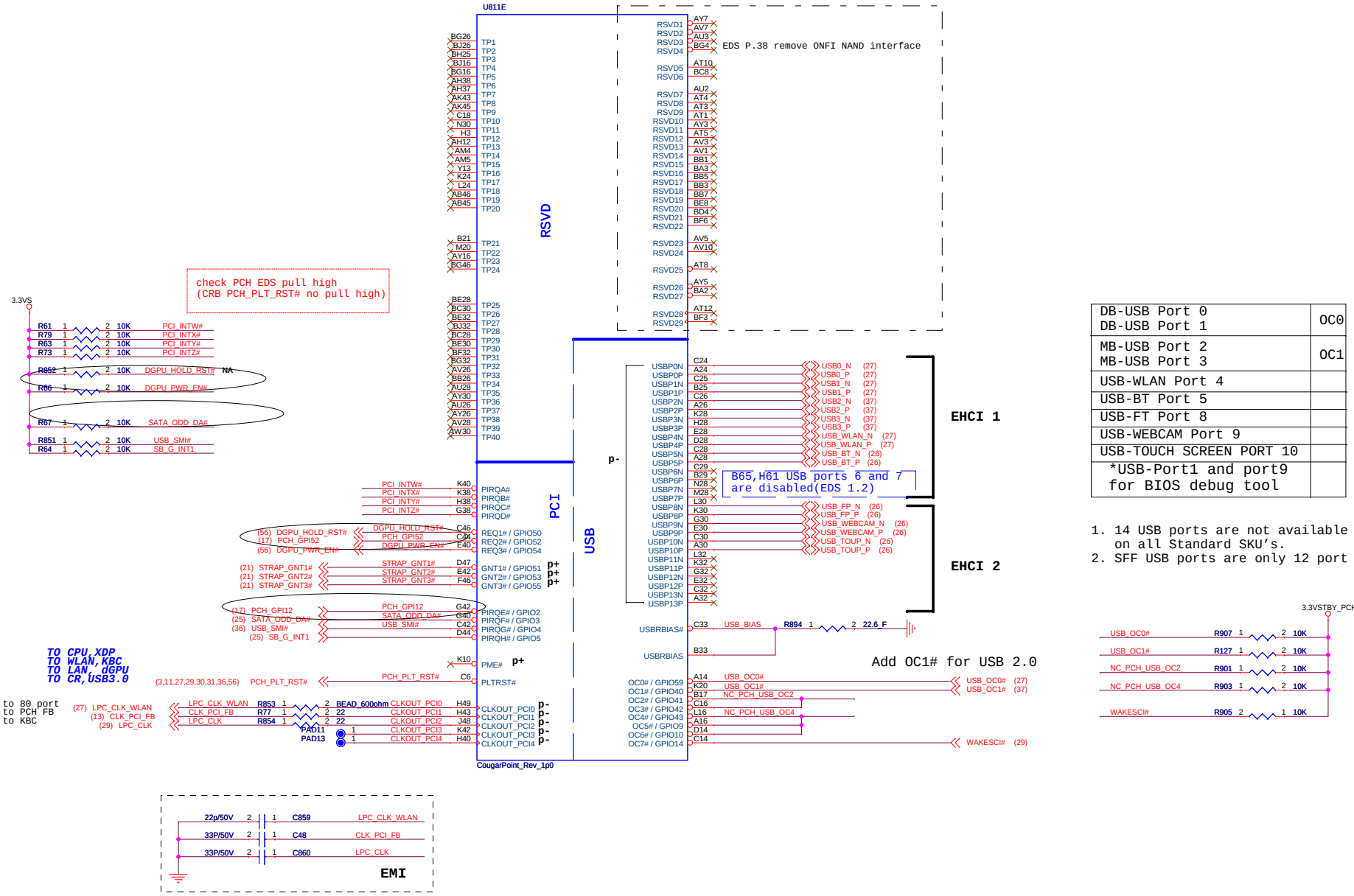
COUGARPOINT (PCI,USB,NVRAM)



DB-USB Port 0 DB-USB Port 1	OC0
MB-USB Port 2 MB-USB Port 3	OC1
USB-WLAN Port 4	
USB-BT Port 5	
USB-FT Port 8	
USB-WEBCAM Port 9	
USB-TOUCH SCREEN PORT 10	
*USB-Port1 and port9 for BIOS debug tool	

1. 14 USB ports are not available on all Standard SKU's.
2. SFF USB ports are only 12 port

FLEX Computing

Project Name : H710DI1	Title : PCH_5/10_PCI_USB_NVRAM
Size :	Document Number : HPMH-40GAB6600-B130 Rev : B
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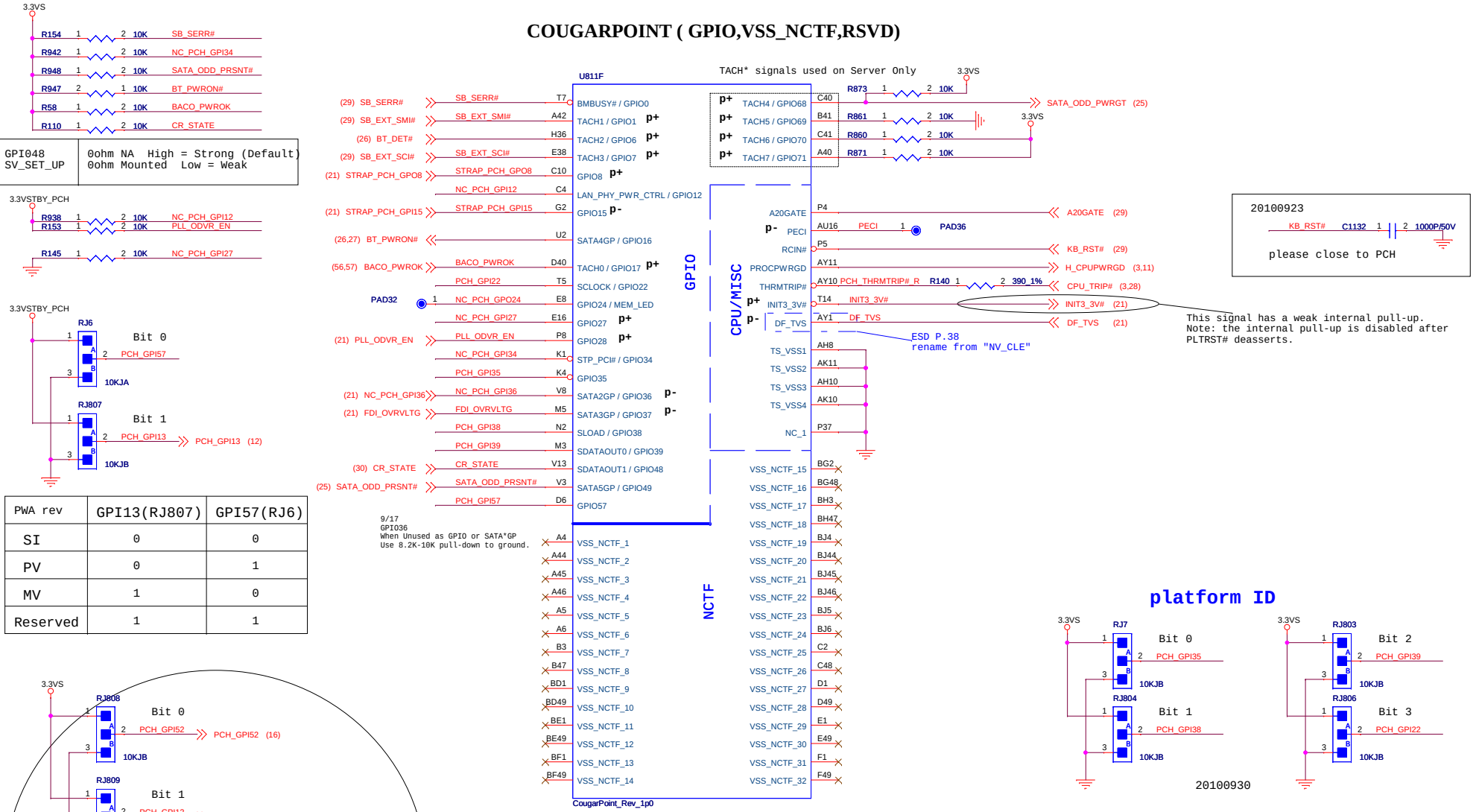
COUGARPOINT (GPIO,VSS_NCTF,RSVD)



PWA rev	GPI13(RJ807)	GPI57(RJ6)
SI	0	0
PV	0	1
MV	1	0
Reserved	1	1

DC or QC HM65 or HM67	GPI12(RJ809) Bit 1	GPI52(RJ808) Bit 0
DC CPU(35W) HM65 PCH	0	0
DC CPU(35W) HM67 PCH	0	1
QC CPU(45W) HM67 PCH	1	0
QC CPU(45W) HM67 PCH	1	1

RJ806	RJ803	RJ804	RJ7	platform	platform ID	SI	PV	
0(B)	0(B)	0(B)	0(B)	Grant 1.0 SG w/ AMD Seymour & Intel Graphic (Beats)	0x1656			
0(B)	0(B)	0(B)	1(A)	Grant 1.0 SG w/ AMD Whistler & Intel Graphic (Beats)	0x1657	SKU4		
0(B)	0(B)	1(A)	0(B)	Grant 1.0 UMA (Beats)	0x1658	SKU2		
0(B)	0(B)	1(A)	1(A)	Grant 1.0 SG w/ AMD Seymour & Intel Graphic (non Beats/Dolby)	0x3581	SKU3		
0(B)	1(A)	0(B)	0(B)	Grant 1.0 SG w/ AMD Whistler & Intel Graphic (non Beats/Dolby)	0x3582			
0(B)	1(A)	0(B)	1(A)	Grant 1.0 UMA (non Beats/Dolby)	0x3583	SKU1		
0(B)	1(A)	1(A)	0(B)	Bogart 1.0 SG w/ AMD Seymour & Intel Graphic+Subwoofer(Beats)	0x1659	SKU5,6		
0(B)	1(A)	1(A)	1(A)	Bogart 1.0 SG w/ AMD Whistler & Intel Graphic+Subwoofer(Beats)	0x165A	SKU7,8		

FLEXComputing

Project Name : H710DI1	Title : PCH_6/10_CPU_GPIO_VSS_RSD	
Size :	Document Number : HPMH-40GAB6600-B130	Rev : B
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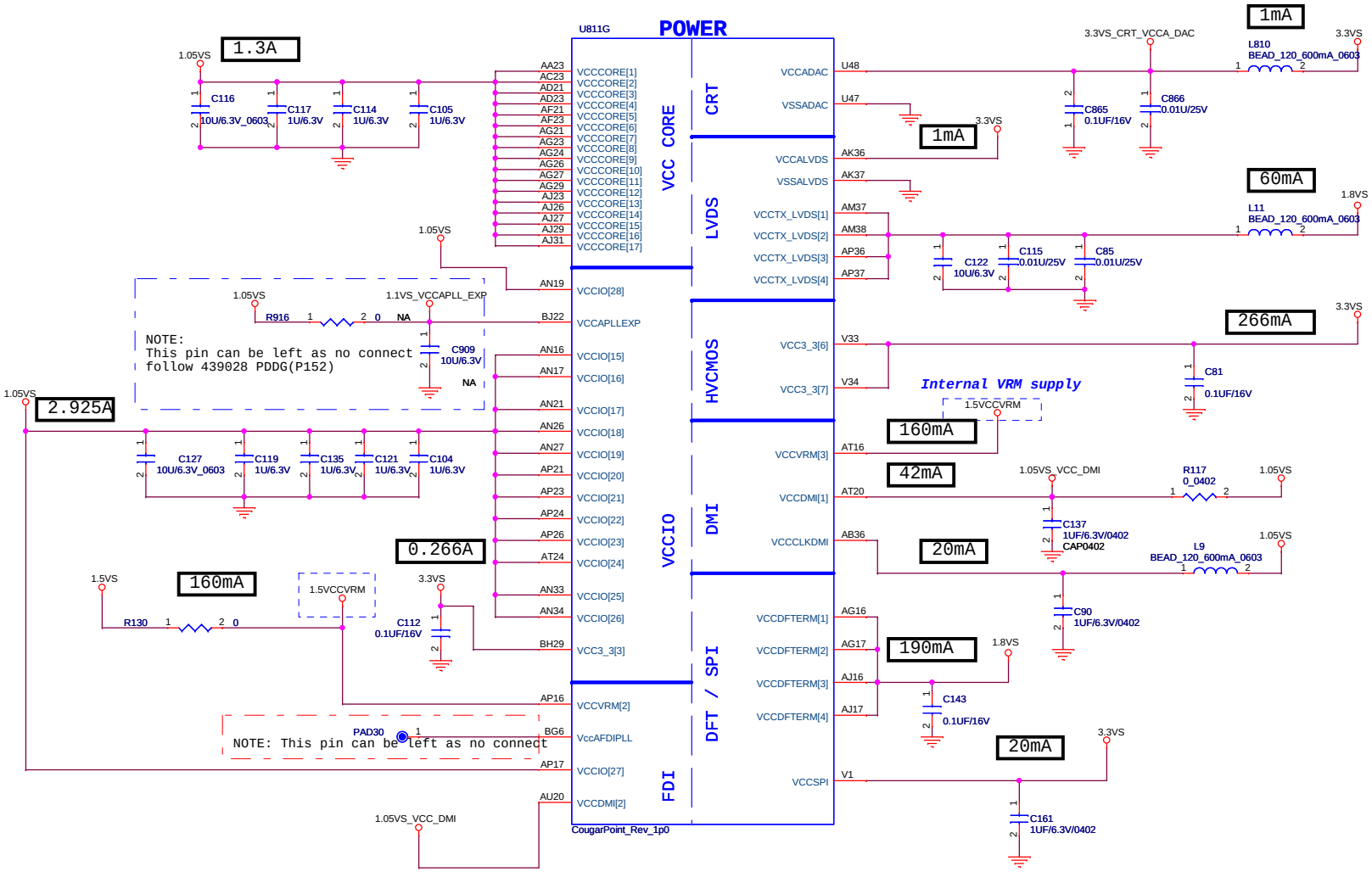
COUGARPOINT (POWER)



FLEX Computing			
Project Name : H710DI1		Title : PCH_7/10_POWER 1	
Size :	Document Number : HPMH-40GAB6600-B130		Rev : B
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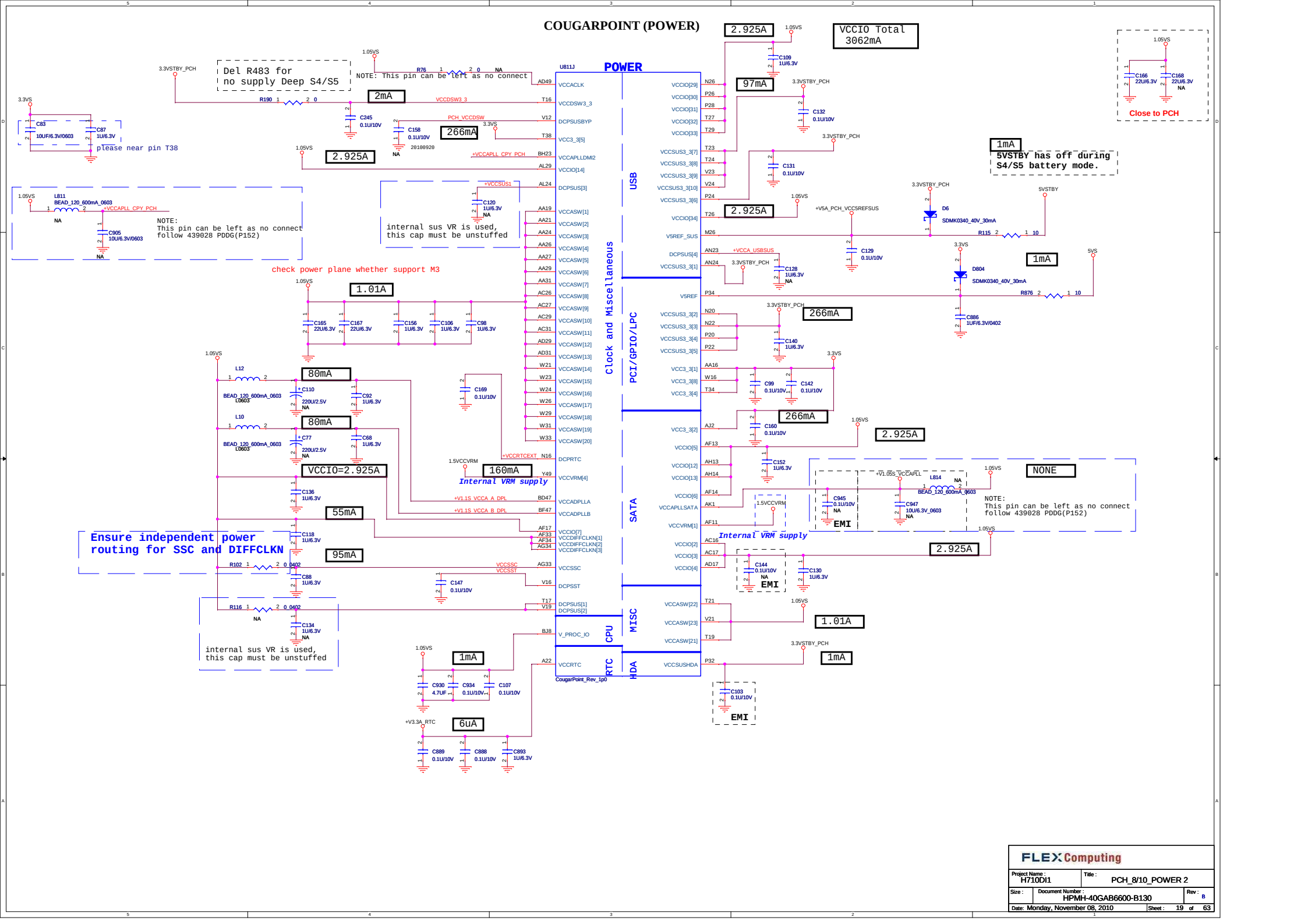
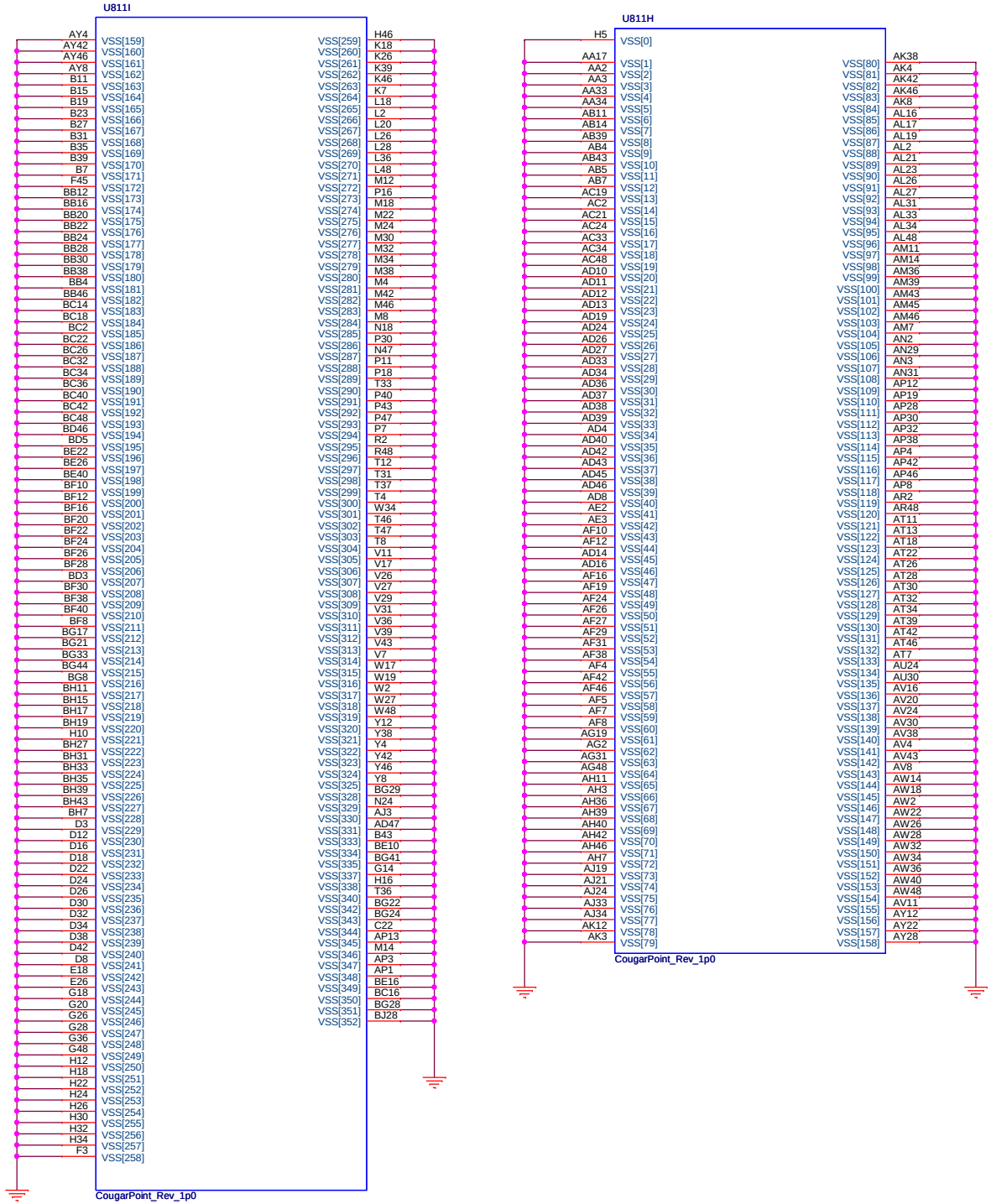
COUGARPOINT (POWER)



COUGARPOINT (GND)



FLEXComputing

Project Name : H710DI1	Title : PCH_9/10_GND	
Size :	Document Number : HPMH-40GAB6600-B130	Rev : B
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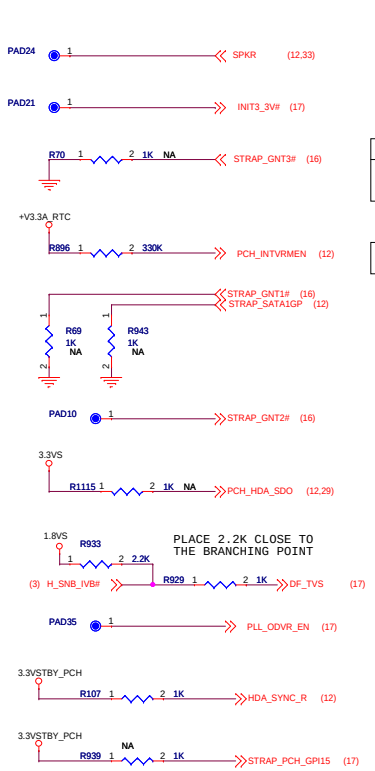
Signal	Usage	When Sampled	Internal PULL	Comment
SPKR	No Reboot	Rising edge of PWROK	Internal PD (The internal PD is disabled after PLTRST# de-asserts)	H: If the signal is sampled high, this indicates that the system is strapped to the No Reboot mode L: Cougar Point will disable the TCO Timer system reboot feature (Chipset Config Registers: Offset (3410h:Bit 5). **Default**
INIT3_3V#	Reserved	Rising edge of PWROK	Internal PU (The internal PU is disabled after PLTRST# de-asserts)	This signal should not be pulled low
GNT[3]#/ GPIO[55]	Top-Block Swap Override	Rising edge of PWROK	Internal PU (The internal PU is disabled after PLTRST# de-asserts)	H: Top Block Swap Mode disabled **Default** L: If the signal is sampled low, this indicates that the system is strapped to the Top Block swap mode
INTVRMEN	Integrated 1.05 V VRM Enable / Disable	Always	NA	H: Integrated 1.05V VRMs enabled **Default** This signal should always be External pulled high L: Integrated 1.05V VRMs disabled
GNT1#/ GPIO51/ SATA1GP/ GPIO19	Boot BIOS Strap bit [1] BBS[1] Boot BIOS Strap bit[0] BBS[0]	Rising edge of PWROK Rising edge of PWROK	Internal PU (The internal PU is disabled after PLTRST# de-asserts) Internal PU (The internal PU is disabled after PLTRST# de-asserts)	GNT1# SATA1GP Boot BIOS Location 0 0 LPC 0 1 Reserved 1 0 PCI 1 1 SPI **Default**
GNT2#/ GPIO53	ESI Strap (Server Only)	Rising edge of PWROK	Internal PU (The internal PU is disabled after PLTRST# de-asserts)	H: Should not be pulled low for desktop and mobile **Default** ESI compatible mode is for server platforms only. L: Configures DMI for ESI compatible operation
HDA_SDO	Flash Descriptor Security Override/ ME Debug Mode	Rising edge of RSMRST#	Internal PD	H: If sampled high,the Flash Descriptor Security will be overridden. L: If strap is sampled low, (Default) the security measures defined in the Flash Descriptor will be in effect. This signal should not be pulled high
DF_TVS	DMI and FDI Tx/ Rx Termination Voltage	Rising edge of PWROK	Internal PD	The internal pull-down is disabled after PLTRST# deasserts
GPIO28	On-Die PLL Voltage Regulator	Rising edge of RSMRST# pin	Internal PU	H: The On-Die PLL voltage regulator is enabled when sampled high **Default** L: When sampled low the On-Die PLL Voltage Regulator is disabled
HDA_SYNC	On-Die PLL Voltage Regulator Voltage Select	Rising edge of RSMRST# pin	Internal PD	H: On-Die PLL VR is supplied by 1.5 V **Default** L: On-Die PLL VR is supplied by 1.8 V
GPIO15	TLS Confidentiality	Rising edge of RSMRST# pin	Internal PD The weak internal pull-down is disabled after RSMRST# deasserts	H: Intel ME Crypto TLS cipher suite with confidentiality L: Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality **Default**
L_DDC_DATA	LVDS Detected	Rising edge of PWROK	Internal PD The internal pull-down is disabled after PLTRST# deasserts.	H:LVDS is detected **Default** L:LVDS is not detected
SDVO_CTRLDATA	Port B Detected	Rising Edge of PWROK	Internal PD (The internal PD is disabled after PLTRST# de-asserts)	H:Port B is detected L:Port B is not detected **Default**
DDPC_CTRLDATA	Port C Detected	Rising edge of PWROK	Internal PD (The internal PD is disabled after PLTRST# de-asserts)	H: Port C is detected L: Port C is not detected **Default**
DDPD_CTRLDATA	Port D Detected	Rising edge of PWROK	Internal PD (The internal PD is disabled after PLTRST# de-asserts)	H: Port D is detected L: Port D is not detected **Default**
DSWVRMEN	Deep S4/S5 Well On-Die Voltage Regulator Enable	Always	NA	If strap is sampled high, the Integrated Deep S4/S5 Well (DSW) On-Die VR mode is enabled.
SATA2GP/ GPIO36	Reserved	Rising edge of PWROK	Internal PD (The internal pull-down is disabled after PLTRST# deasserts.)	NOTE: This signal should not be pulled high when strap is sampled.
SATA3GP/ GPIO37	Reserved	Rising edge of PWROK	Internal PD (The internal pull-down is disabled after PLTRST# deasserts.)	NOTE: NOTE: This signal should not be pulled high when strap is sampled.
GPIO8	Reserved	Rising edge of RSMRST#	Internal PU (Pull-up is disabled after RSMRST# is deasserted.)	NOTE: This signal should not be pulled low



NO REBOOT	
NA	Low=Disable(Default)
MOUNTED	High=Enable

A16 swap override Strap	
STP_A16OVR	Low = A16 swap override High = Default

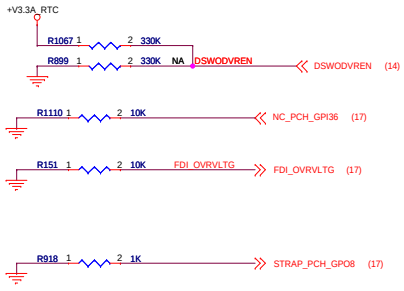
INTVRMEN- Integrated SUS 1.05V VRM Enable

Flash Descriptor Security Overide		
PCH_HDA_SDO	NA	Low=Disable(Default)
	MOUNTED	High=Enable

DMI & FDI Termination Voltage	
DF_TVS	Set to Vss when LOW Set to Vcc when HIGH

PLL ON DIE VR ENABLE	
PLL_ODVR_EN	ENABLE- UNSTUFF DISABLE-STUFF

HR only support 1.5 V
HDA_SYNC need PU to HDA SUS rail through 1k ohm for 451710_451710 SPEC



DSWODVREN - On Die DSW VR Enable	
Pull High	Enable (Default)
Pull Down	Disable

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36	LOW - Tx, Rx terminated to same voltage (DC Coupling Mode) DEFAULT

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Mode) DEFAULT

GPIO8 Integrated Clock Chip Enable
High : Disable Low : Enable(default)

FLEXComputing

Project Name : H710DI1	Title : PCH_10/10_STRAP	
Size :	Document Number : HPMH-40GAB6600-B130	Rev : B
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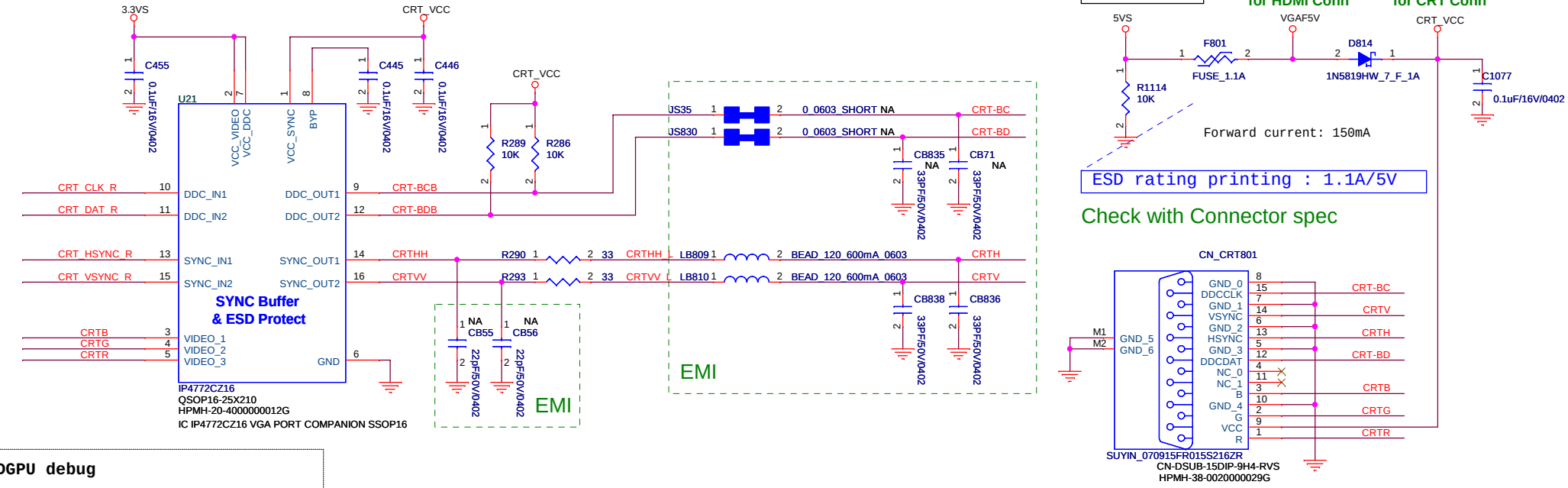
D-Sub



5V/1.1A

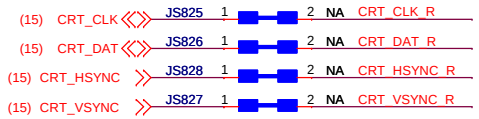
for HDMI Conn

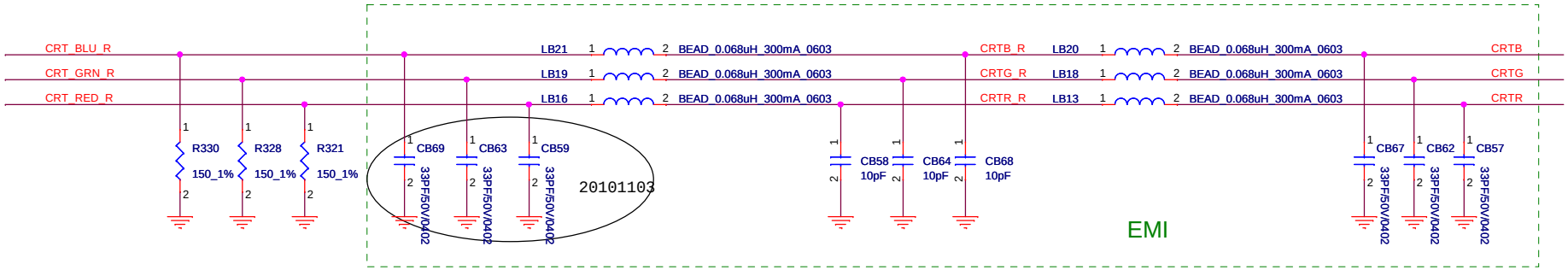
for CRT Conn

ESD rating printing : 1.1A/5V

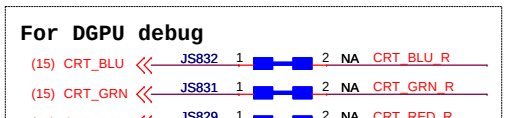
Check with Connector spec

For DGPU debug





For DGPU debug



FLEXComputing

Project Name : H710DI1	Title : CRT CONN	
Size :	Document Number : HPMH-40GAB6600-B130	Rev : B
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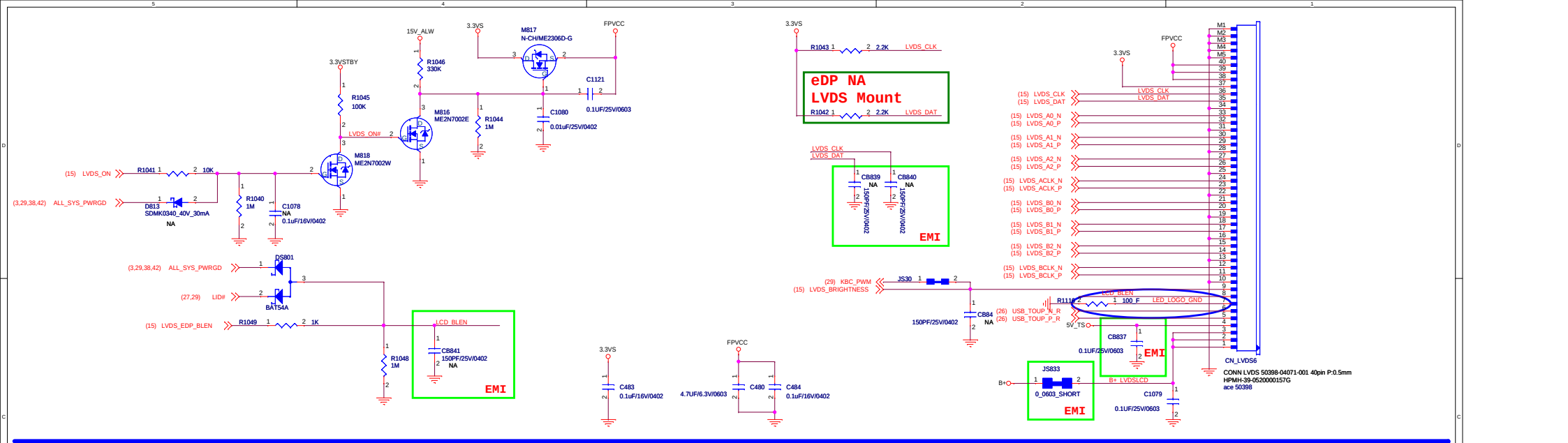

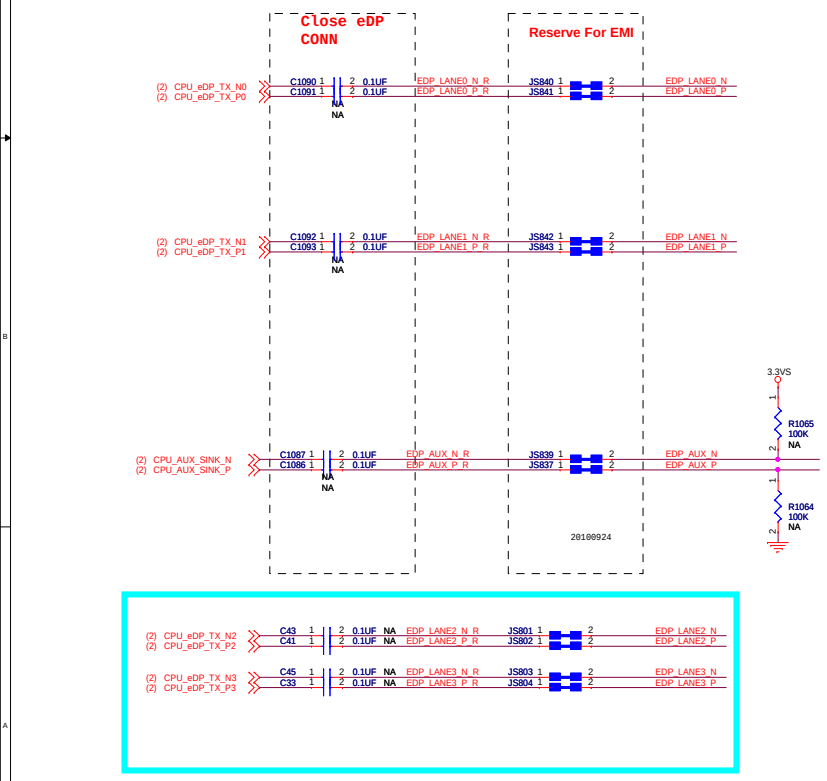

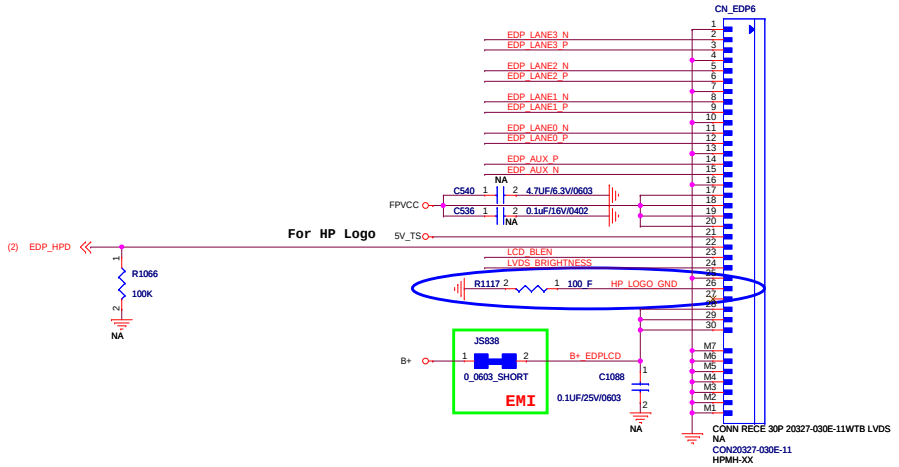

1. Check pin definition of eDP panel spec.
2. Confirm connector PN

FLEXComputing

Project Name : H710DI1	Title : eDP_LVDS CONN_HP Logo
Size :	Document Number : HPMH-40GAB6600-B130 — Rev : B
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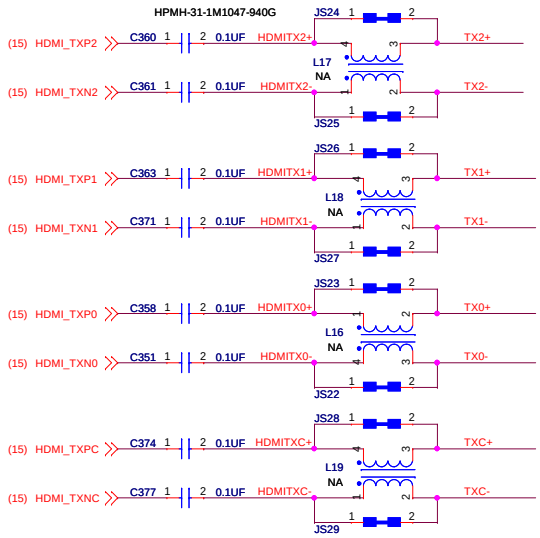
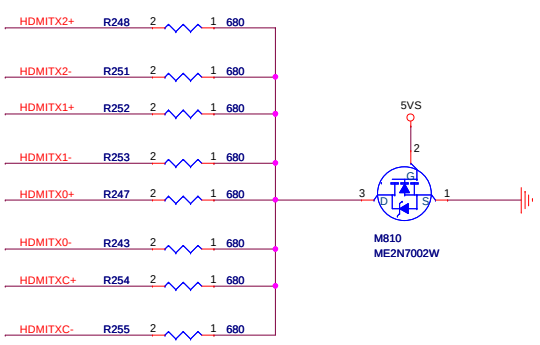
HDMI

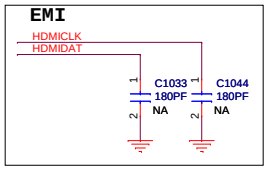
CLOSE to CN_HDMI1

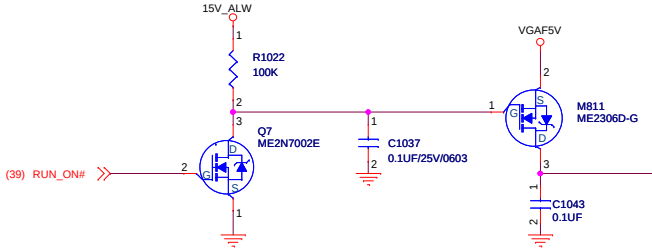
HPMH-32-4000000104G

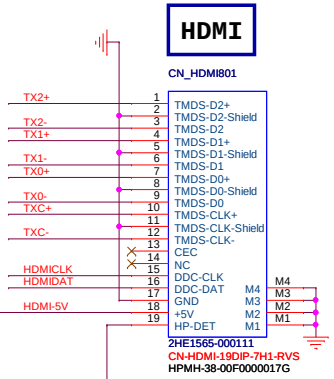
Intel Huron River: 680 ohm
AMD Danube: 715 ohm
AMD Sabine: 715 ohm

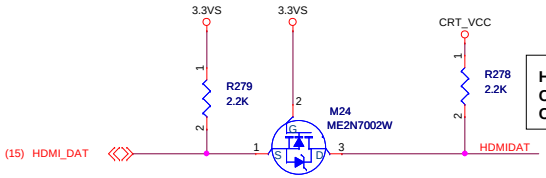




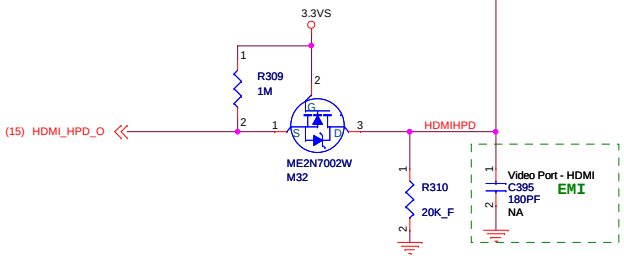


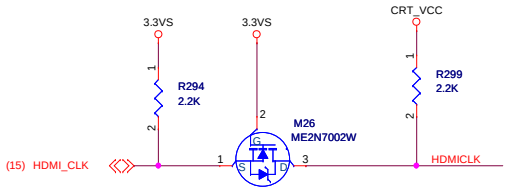






HDMI test
C1 -- Cp=45pf
C2 -- Cp=46pf (spec<50pf)





FLEX Computing

Project Name : H710DI1	Title : HDMI CONN
Size : Custom	Document Number : HPMH-40GAB6600-B130 Rev : B
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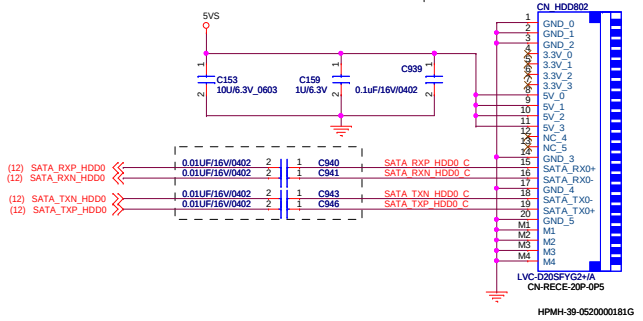
HDD

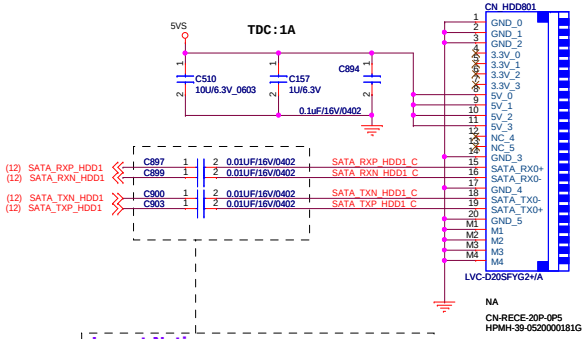
Layout Notice:
0.01uF series cap close to connector
follow SATA Signal Connection Checklist



2nd HDD

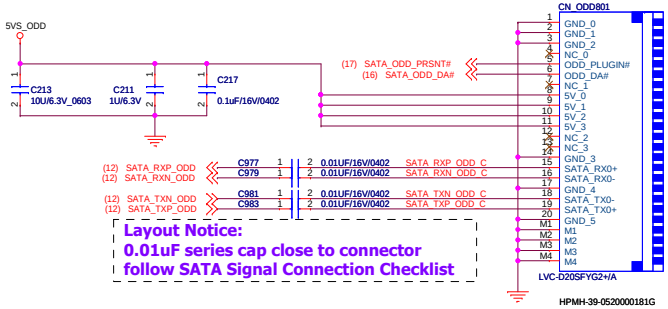
FOR 17" MB USE WTB CONNECTOR

CONN SPEC:0.3A/PIN



Layout Notice:
0.01uF series cap close to connector
follow SATA Signal Connection Checklist

ODD



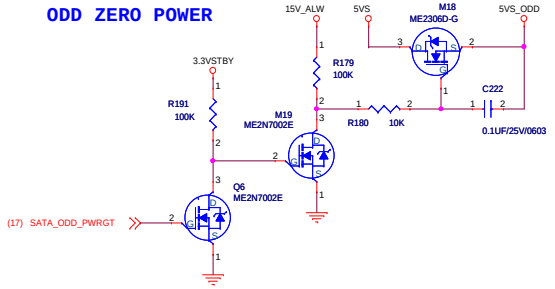
Layout Notice:
0.01uF series cap close to connector
follow SATA Signal Connection Checklist

TDC:2A

Change to Cable type Conn

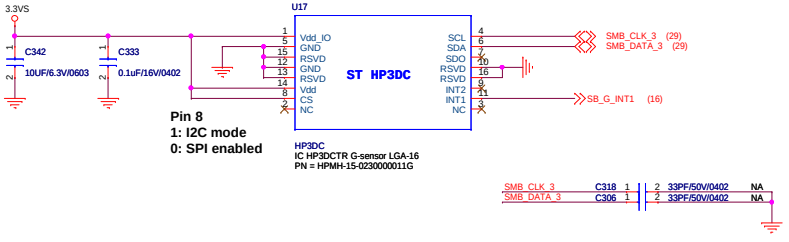
ODD Zero Power

Check if meet max current!!

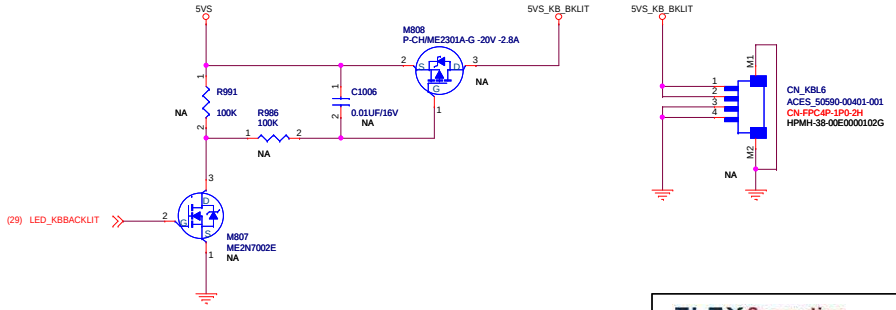


G-Sensor

G-SENSOR
ST HP3DC
3.3VS
ADDR: 0011000x(30h) - SDO PD
ADDR: 0011010x(32h) - SDO NC
SINK: ??mA@Vol=0.33V(MAX)



KB Backlit



FLEXComputing

Project Name : H710DI1	Title : HDD_ODD_G-Sensor_KB BKL
Size :	Document Number : HPMH-40GAB6600-B130 Rev : B
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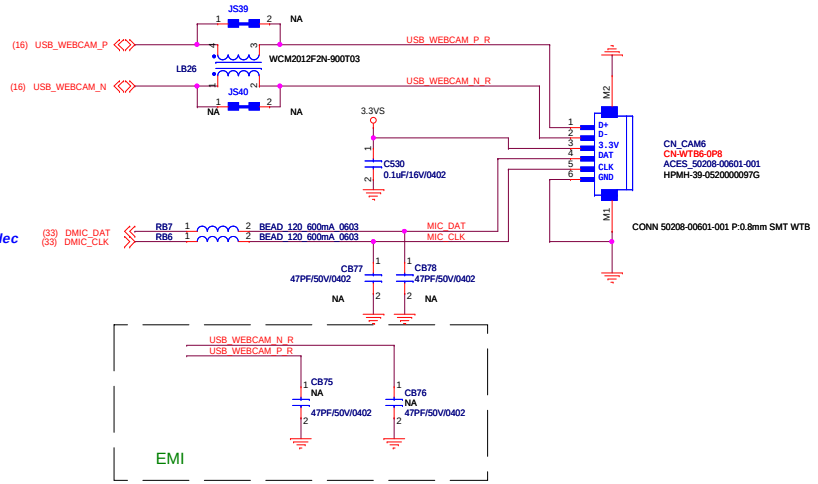
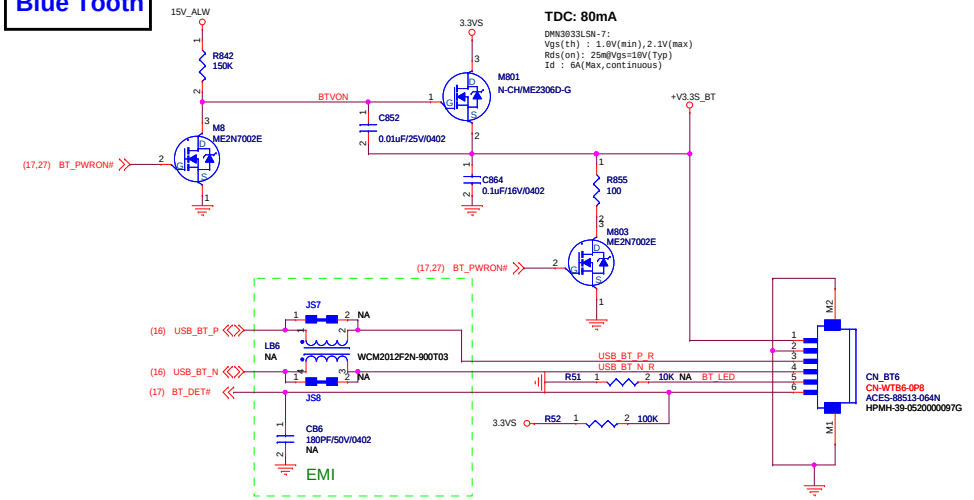
Web CAM



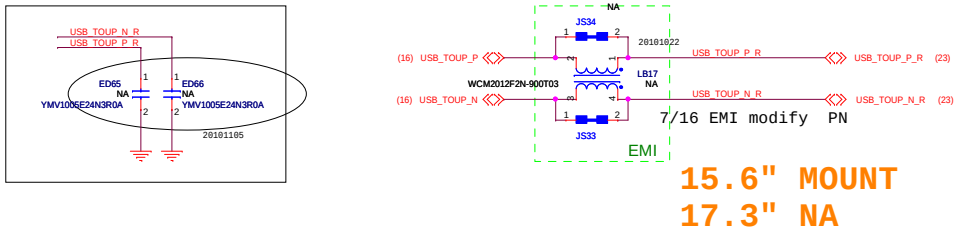
Blue Tooth



TouchScreen
(Module CONN)

Touch Screen power is 5V type

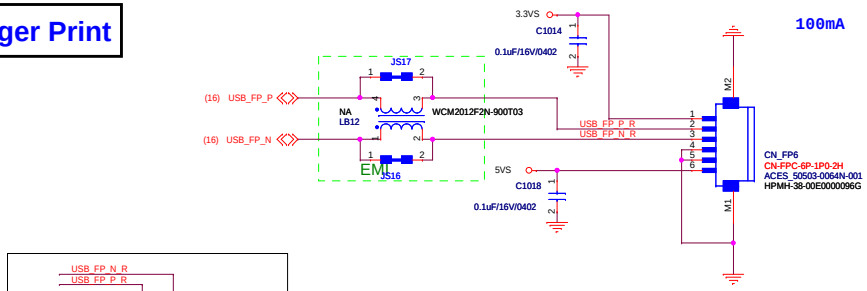
Peak 200mW 40mA

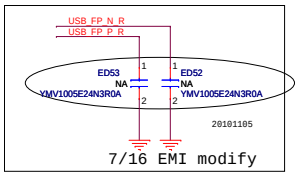


15.6" MOUNT
17.3" NA

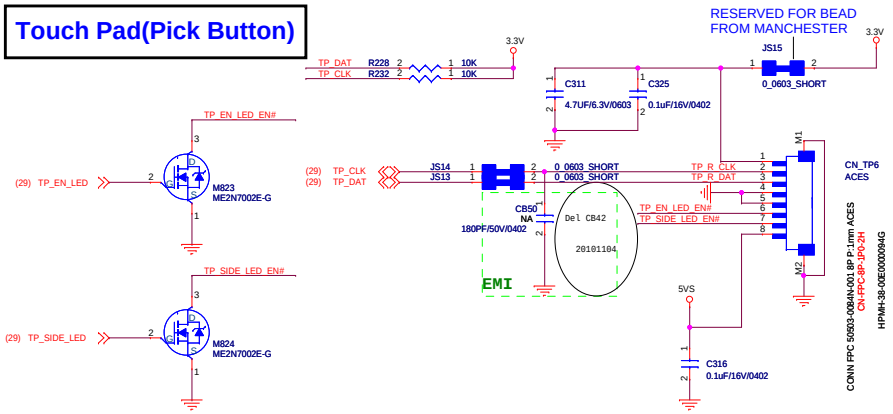
Finger Print

100mA

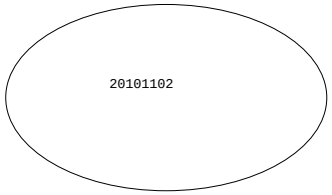




Touch Pad(Pick Button)



LID



FLEXComputing

Project Name : H710DI1	Title : WebCAM_BT_FP_TS_TP_LID
Size :	Document Number : HPMH-40GAB6600-B130 Rev : B
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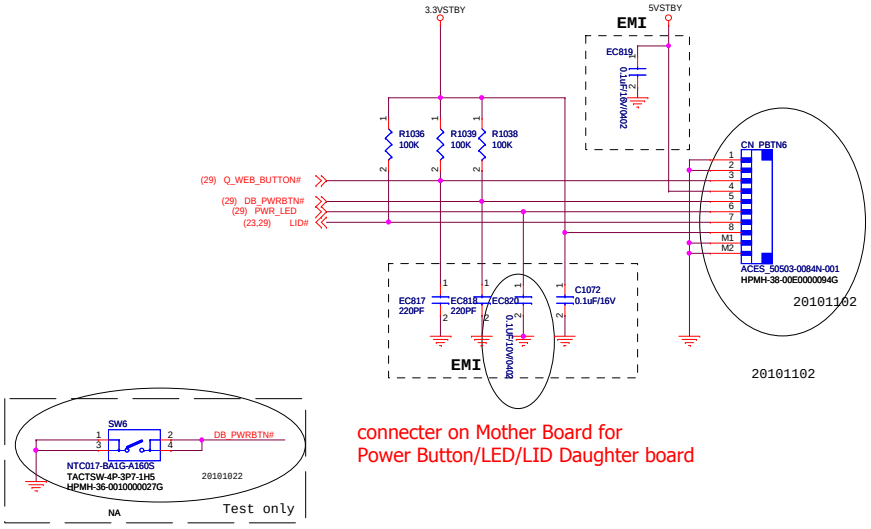
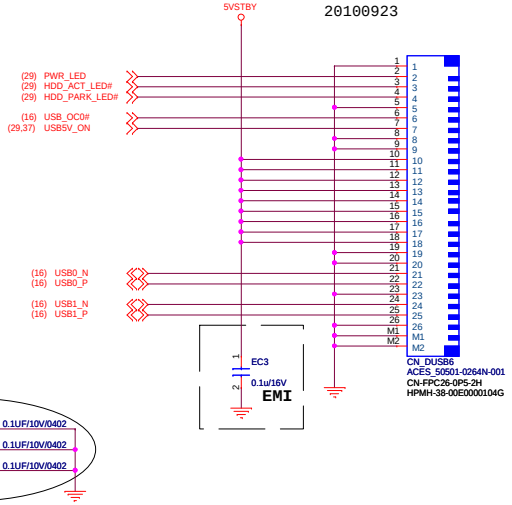
PWRBTN BOARD

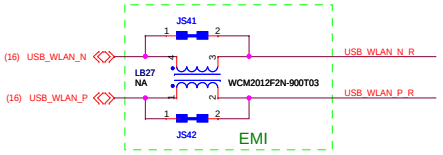


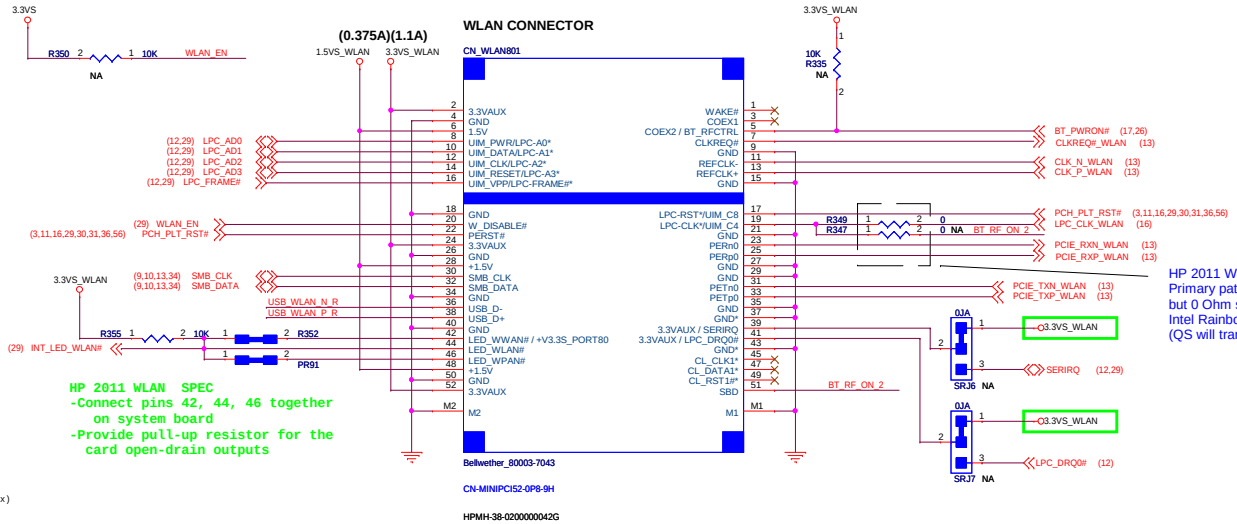
connecter on Mother Board for
Power Button/LED/LID Daughter board

USB BOARD

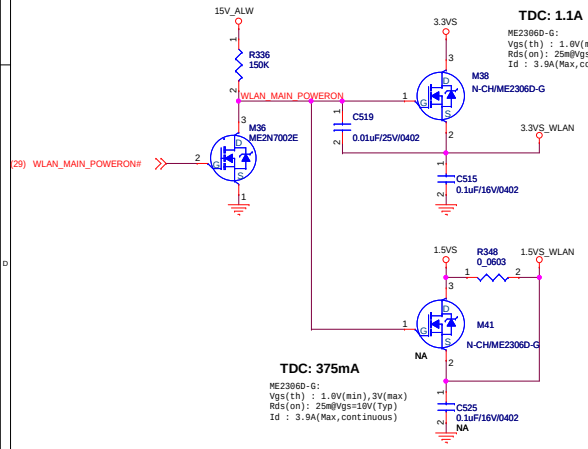


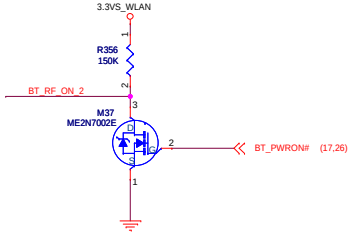
Mini-PCIE - WLAN (Half size)

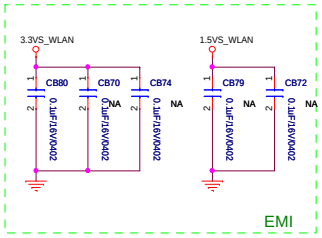




HP 2011 WLAN SPEC 2'nd RF ON/OFF Pin Primary path is to implement it on pin 51, but 0 Ohm strap to pin 19 required for Intel Rainbow Peak ES2 cards use (QS will transition to pin 51).







FLEX Computing

Project Name : H710D1	Title : MB to DB CONN_WLAN
Size :	Document Number : HPMH-40GAB6600-B130 Rev : B
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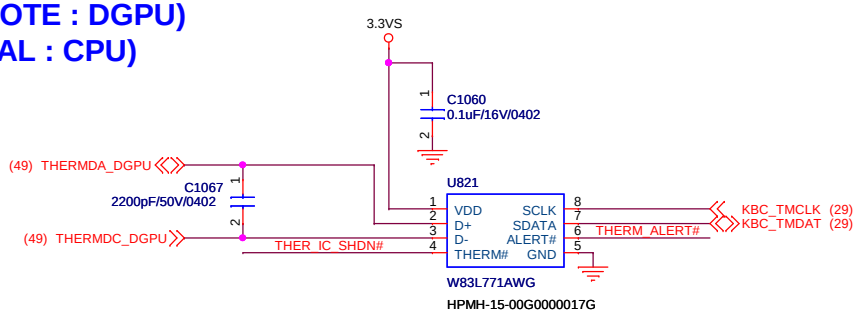
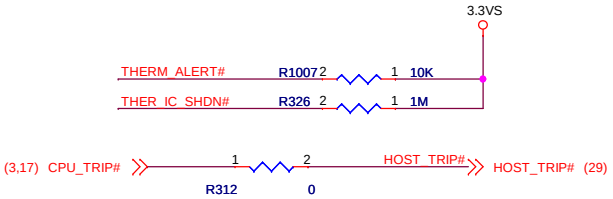
Thermal Sensor
(REMOTE : DGPU)
(LOCAL : CPU)



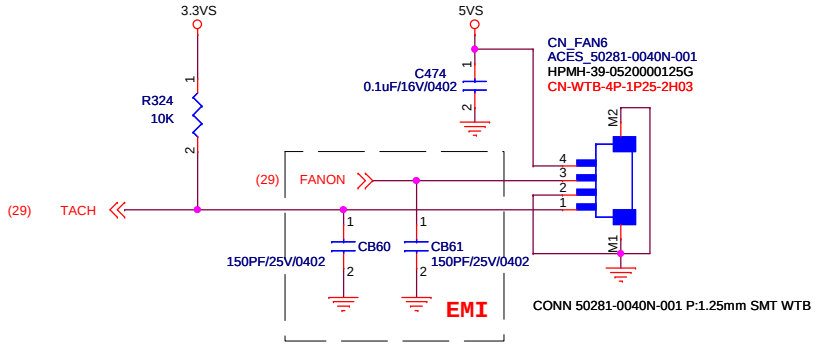
Place between CPU and VGA



THERMAL IC FOR CPU or DGPU

WINBOND	W83L771AWG	ODMH-15-00G0000017G 1001100x(98h)
ON SEMI	ADT7421ARMZ-REEL	???
GMT	G780P81U	???

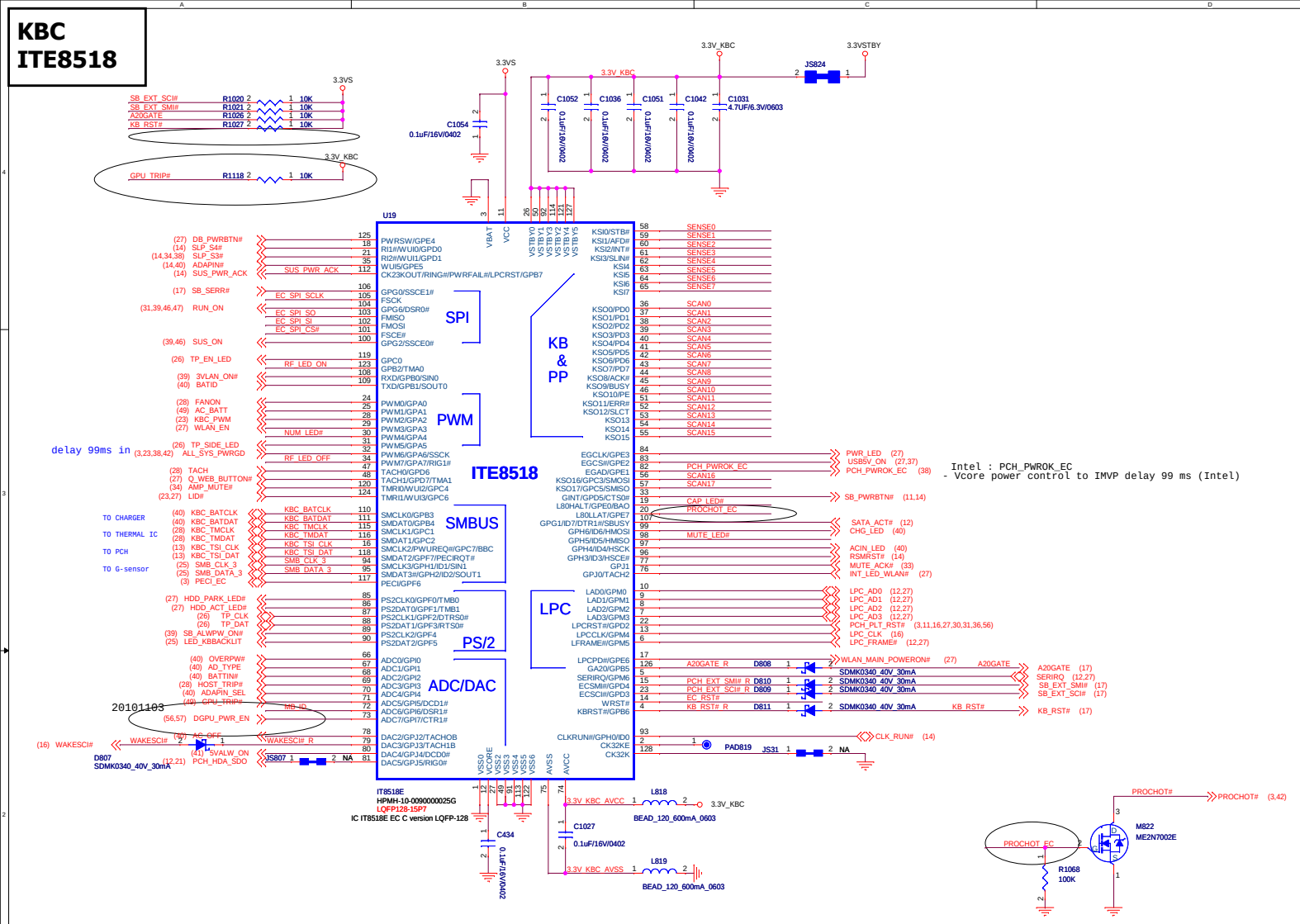
FAN CONN



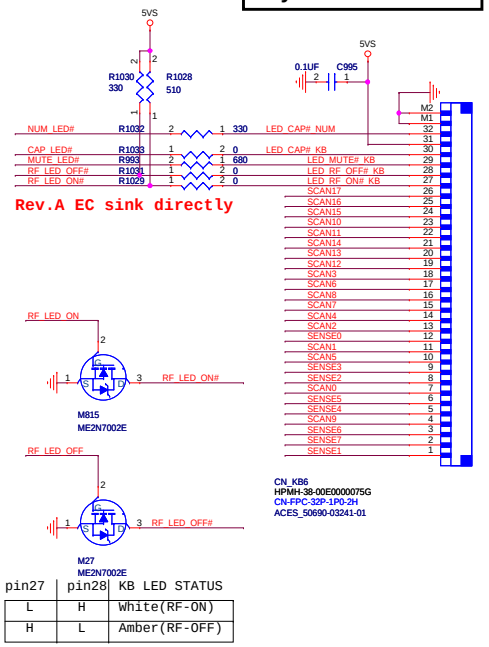
FLEXComputing

Project Name : H710DI1	Title : THERM IC_FAN	
Size :	Document Number : HPMH-40GAB6600-B130	Rev : B
Date: Monday, November 08, 2010	Sheet : 28 of 63	

KBC ITE8518

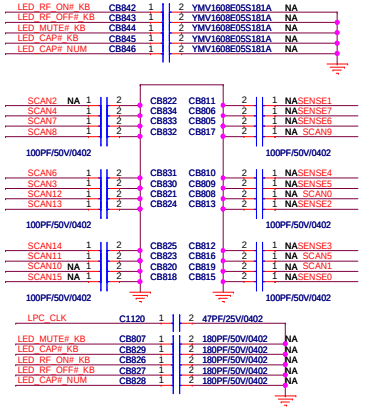


Keyboard Connector

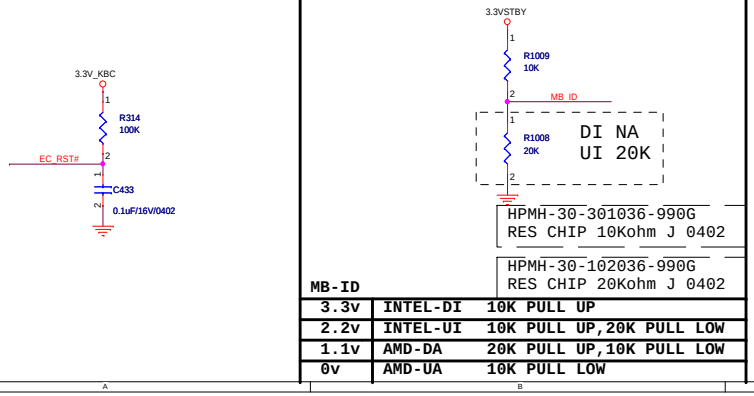


pin27	pin28	KB LED STATUS
L	H	White(RF-ON)
H	L	Amber(RF-OFF)

EMI

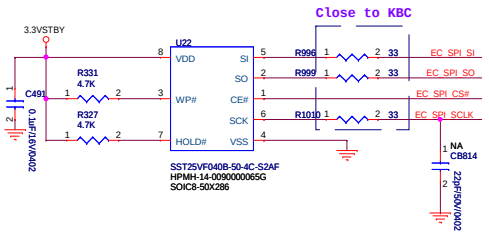


Board ID

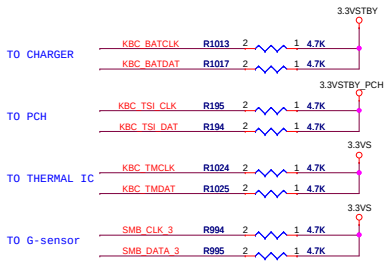


MB-ID		
3.3v	INTEL-DI	10K PULL UP
2.2v	INTEL-UI	10K PULL UP,20K PULL LOW
1.1v	AMD-DA	20K PULL UP,10K PULL LOW
0v	AMD-UA	10K PULL LOW

SPI ROM (512KB)

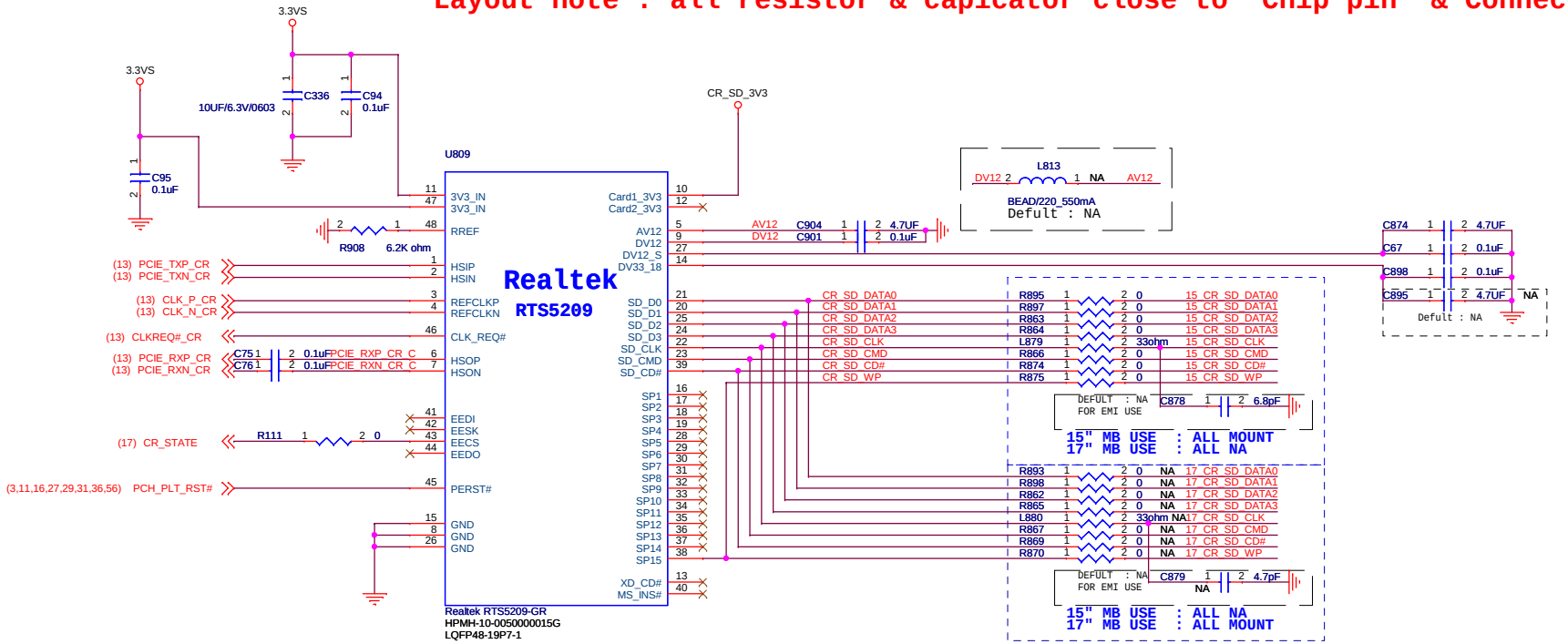


SM BUS

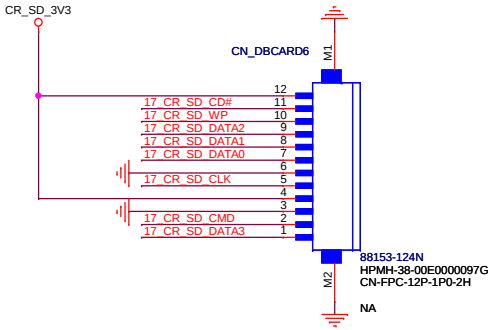


Card Reader

Layout note : all resistor & capicator close to Chip pin & Connector pin



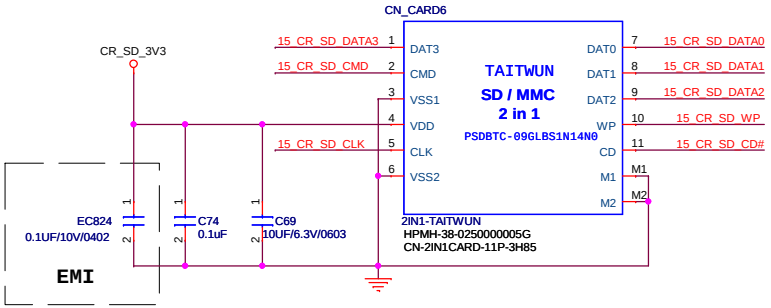
FOR 17" MB USE WTB CONNECTOR



FOR 15" MB ALL COMPONENT : NA

FOR 17" MB ALL COMPONENT : MOUNT

FOR 15" MB USE CardReader CONNECTOR



FOR 15" MB ALL COMPONENT : MOUNT

FOR 17" MB ALL COMPONENT : NA

FLEX Computing

Project Name : H710DI1	Title : Card Reader (R5U220)
Size :	Document Number : HPMH-40GAB6600-B130 — Rev : B
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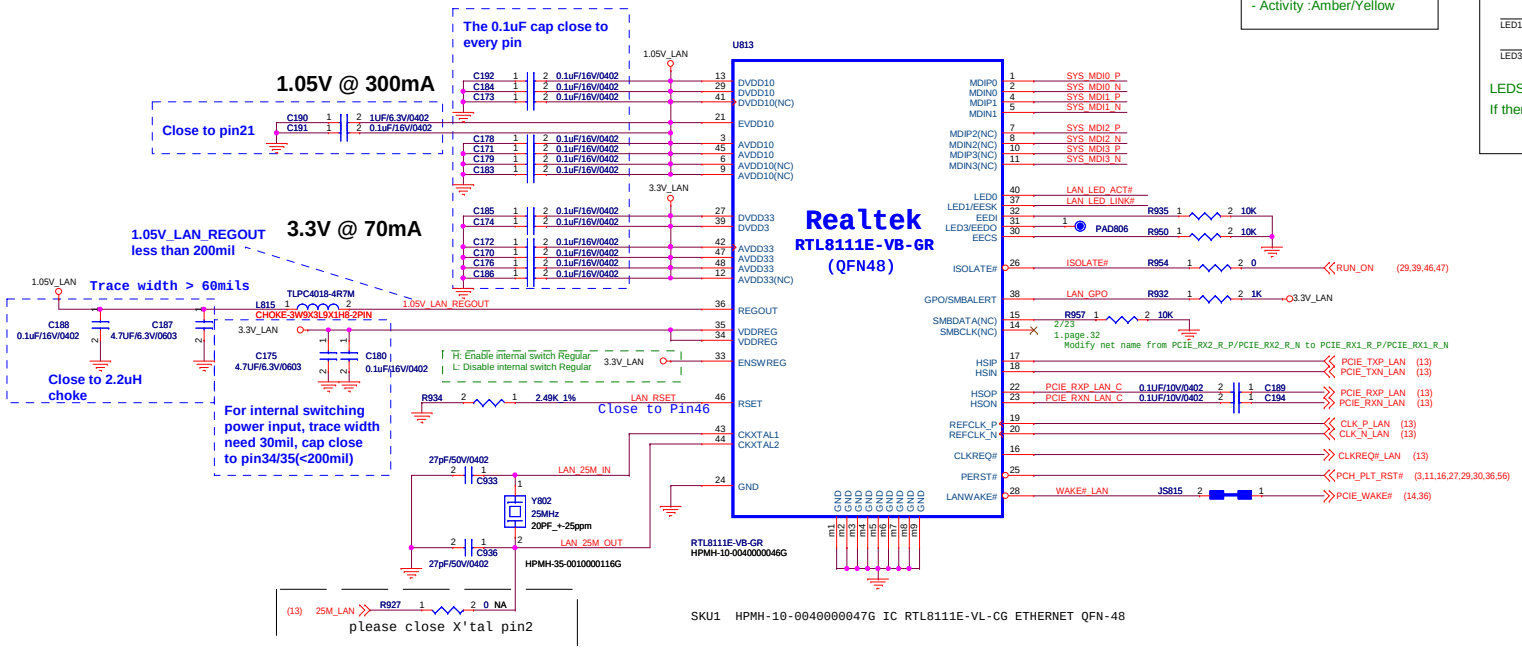
GBit LAN Controller

Mini-spec requirements:
10/100/1000 :
- Link :White
- Activity :Amber/Yellow

RTL8111E

LEDS1-0	00	01	10	11
LED0	ACT ALL	LINK ALL /ACT ALL	LINK10 /ACT ALL	LINK10 /ACT10
LED1	LINK100	LINK100	LINK100	LINK100 /ACT100
LED3	LINK1000	LINK1000	LINK1000	LINK1000 /ACT1000

LEDS1-0s initial value comes from the EEPROM
If there is no EEPROM, the default value is 11



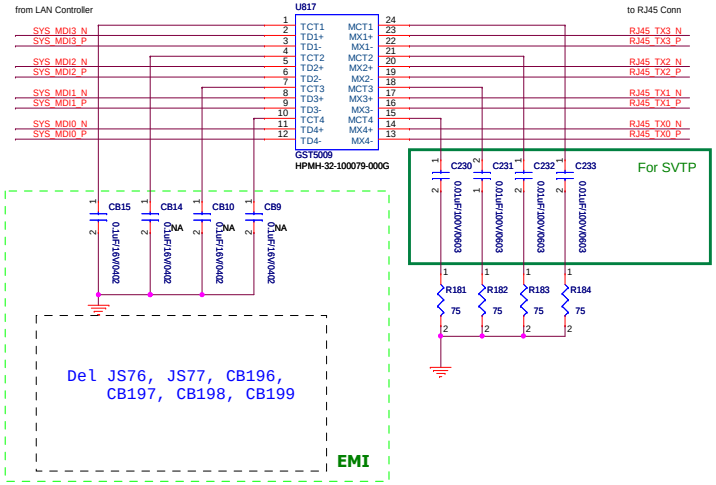
SKU1 HPMH-10-0040000047G IC RTL8111E-VL-CG ETHERNET QFN-48

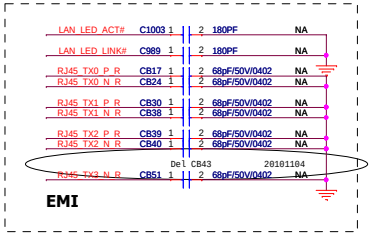
TRANSFORMER

2009.09.22 ref. "RTL8102E_8111D 48PIN demo_board v200_2008.04.30"

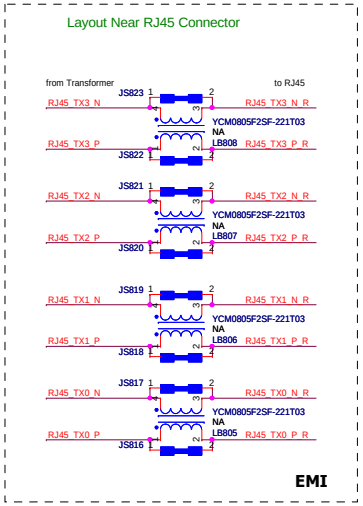
Transformer :
Gbit P/N: 32-100079-000G(GST5009)
10/100 P/N: 32-0000000009G (TST1284)

Layout near RJ45 Connector

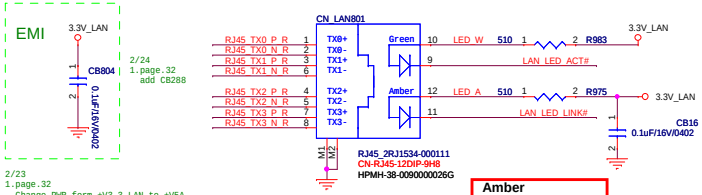




Layout Near RJ45 Connector



RJ45 Cable Connector



Reference:
RJ45 Phone Jack
Pin define:
1 TXD+0
2 TXD-0
3 TXD+1
4 TXD+2
5 TXD-2
6 TXD-1
7 TXD+3
8 TXD-3

SVTP_v4.03
2.6 - Ethernet Checklist - Rev C.xls

- Ch.3.1.4.4
Some older cheap RJ-45s only populate pins 1,2,3,6. 10/100 requires the other 4 pins for grounding. Gigabit Ethernet requires all 8 pins for data signals.

- Ch.3.1.4.13
Resistance from RJ-45 shell to any other chassis ground point (ohms) less than 1 ohm

- Ch.3.1.4.14 & Ch.3.1.4.15
Protection against non-standard power-over-Ethernet (PoE) : Resistance between pins 1,3 (TXD0P,TXD1P) and pins 4,7 (TXD2P,TXD3P) of the RJ-45 greater than 58K ohms.

FLEXComputing

Project Name : H710DI1	Title : RJ45_LAN (RTL8111E-VB-GR)	
Size : C	Document Number : HPMH-40GAB6600-B130	Rev : B
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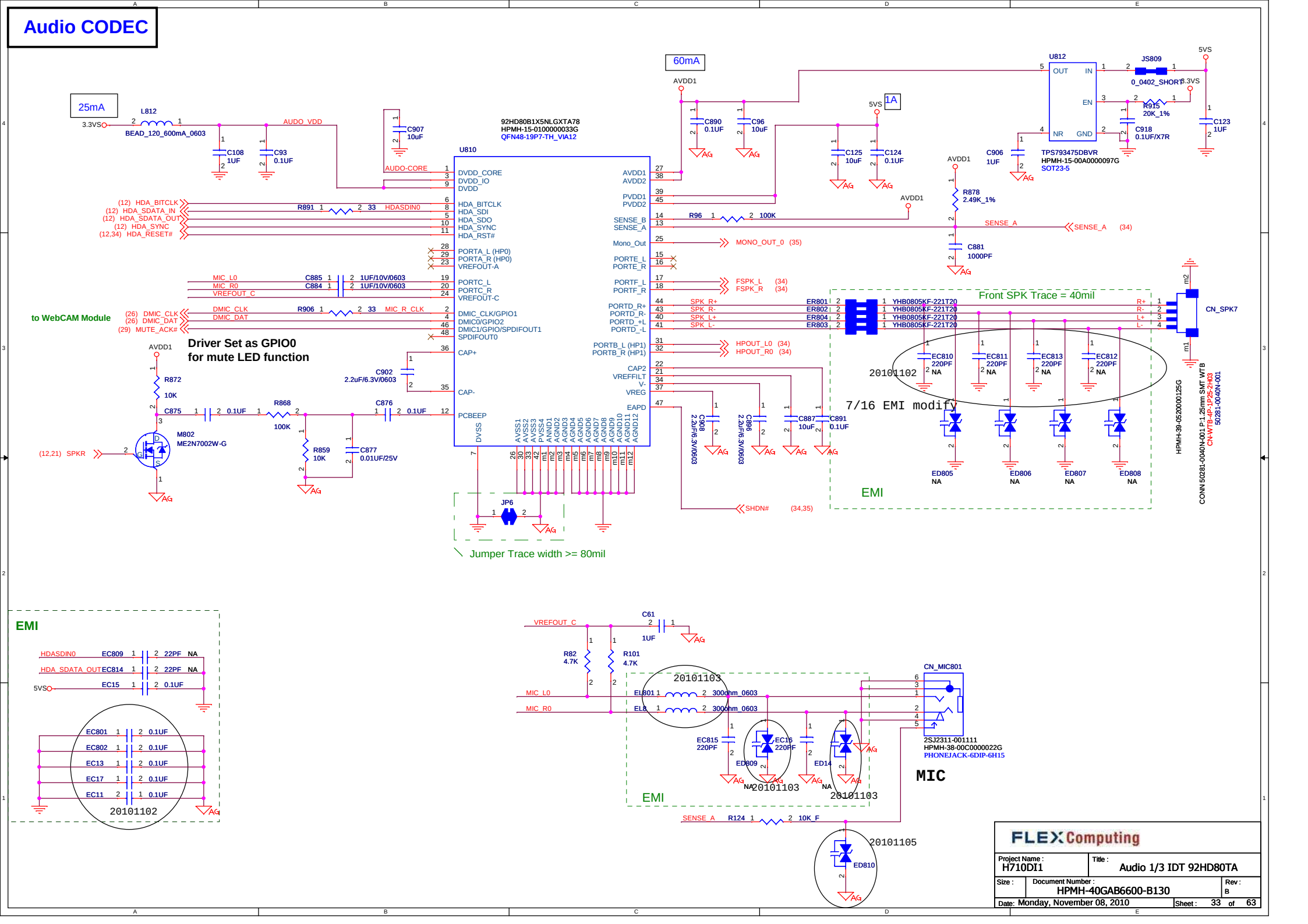
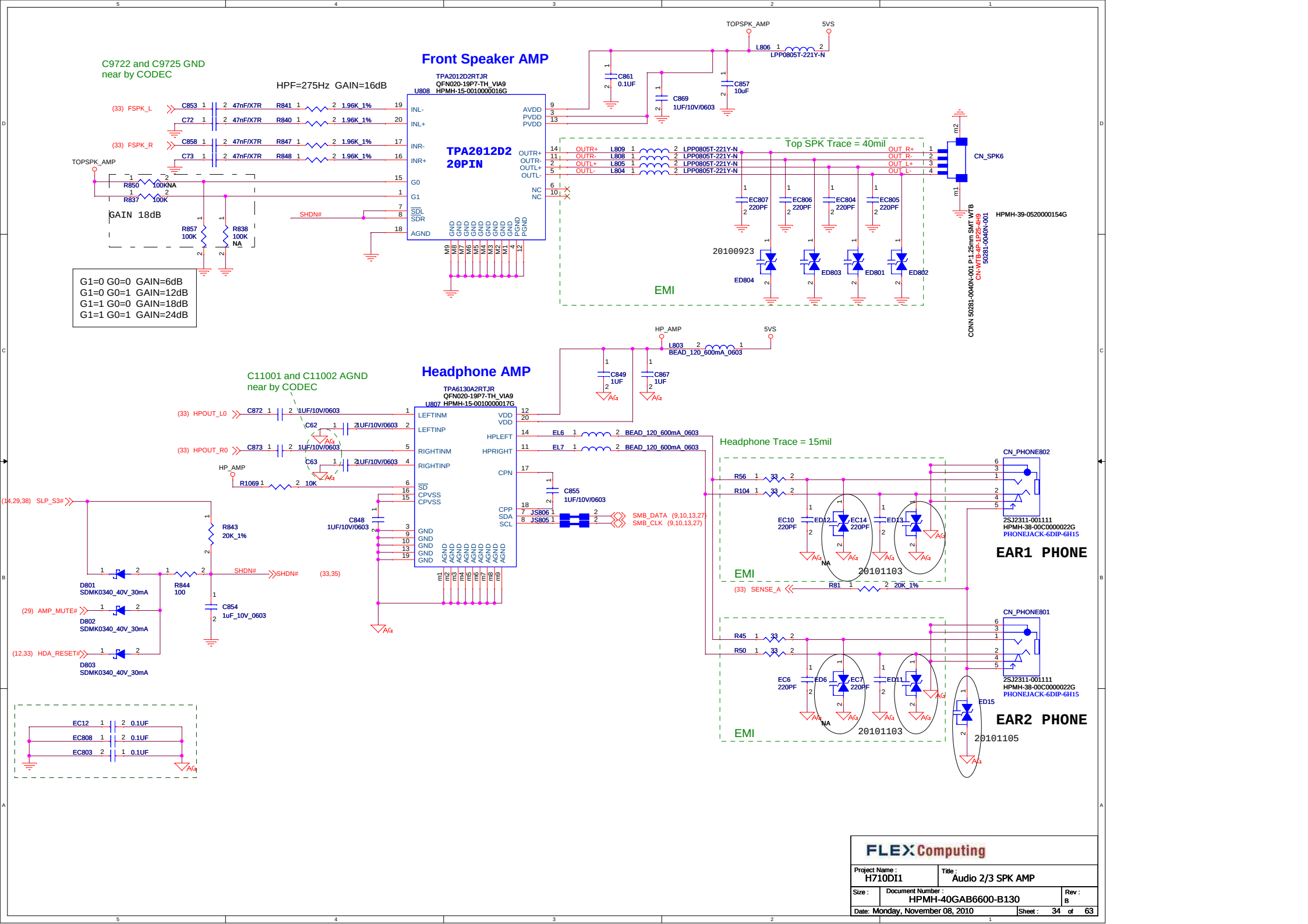
FLEX Computing

Project Name : H710DI1	Title : RESERVE	
Size :	Document Number : HPMH-40GAB6600-B130	Rev : B
Date: Monday, November 08, 2010	Sheet : 32 of 63	

Audio CODEC



FLEX Computing			
Project Name : H710DI1	Title : Audio 1/3 IDT 92HD80TA		
Size :	Document Number : HPMH-40GAB6600-B130		Rev : B
Date: Monday, November 08, 2010		Sheet : 33 of 63	



FLEX Computing			
Project Name : H710DI1		Title : Audio 2/3 SPK AMP	
Size :	Document Number : HPMH-40GAB6600-B130		Rev : B
Date: Monday, November 08, 2010		Sheet : 34 of 63	

If without supply Woofer all page NA

WOOFER AMP

HPA00836PWPR
HTSSOP28-25P6X220-TH
U805

HPA00836PWPR
28PIN

C9742 GND
near by CODEC

GAIN 20dB

G1=0 G0=0	GAIN=20dB
G1=0 G0=1	GAIN=26dB
G1=1 G0=0	GAIN=32dB
G1=1 G0=1	GAIN=36dB

Woofer SPK Trace = 40mil

Kevin modify-0909

IC TLV2464CPWR Audio AMP TSSOP-14

Always NA

FLEX Computing	
Project Name : H710DI1	Title : Audio 3/3 WOOFER AMP
Size :	Document Number : HPMH-40GAB6600-B130 Rev : B
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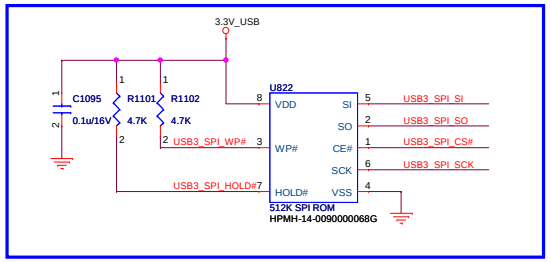
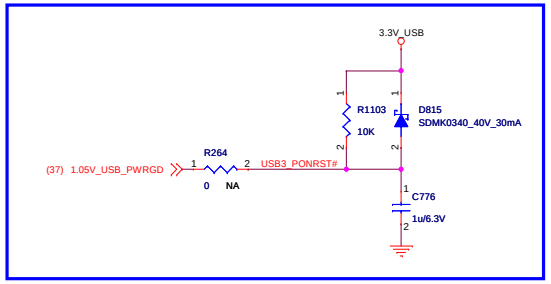
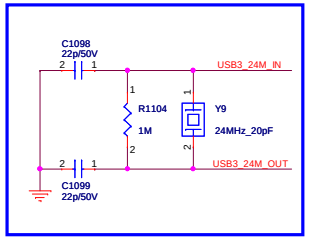
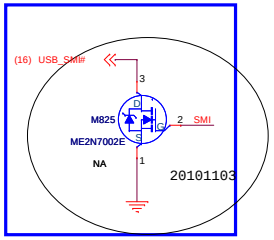
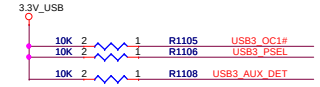
USB3.0 NEC uDP720200

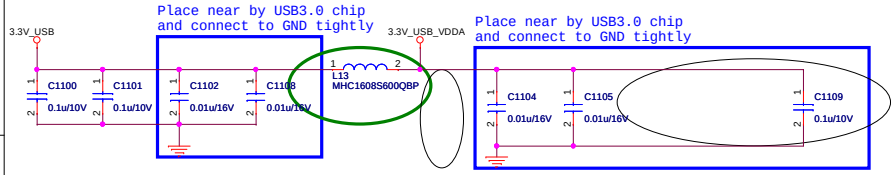


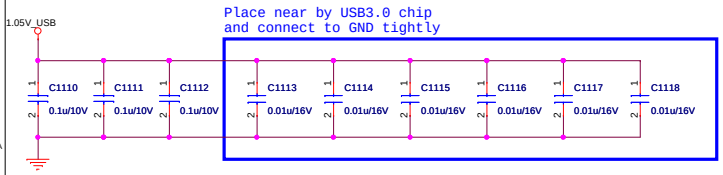


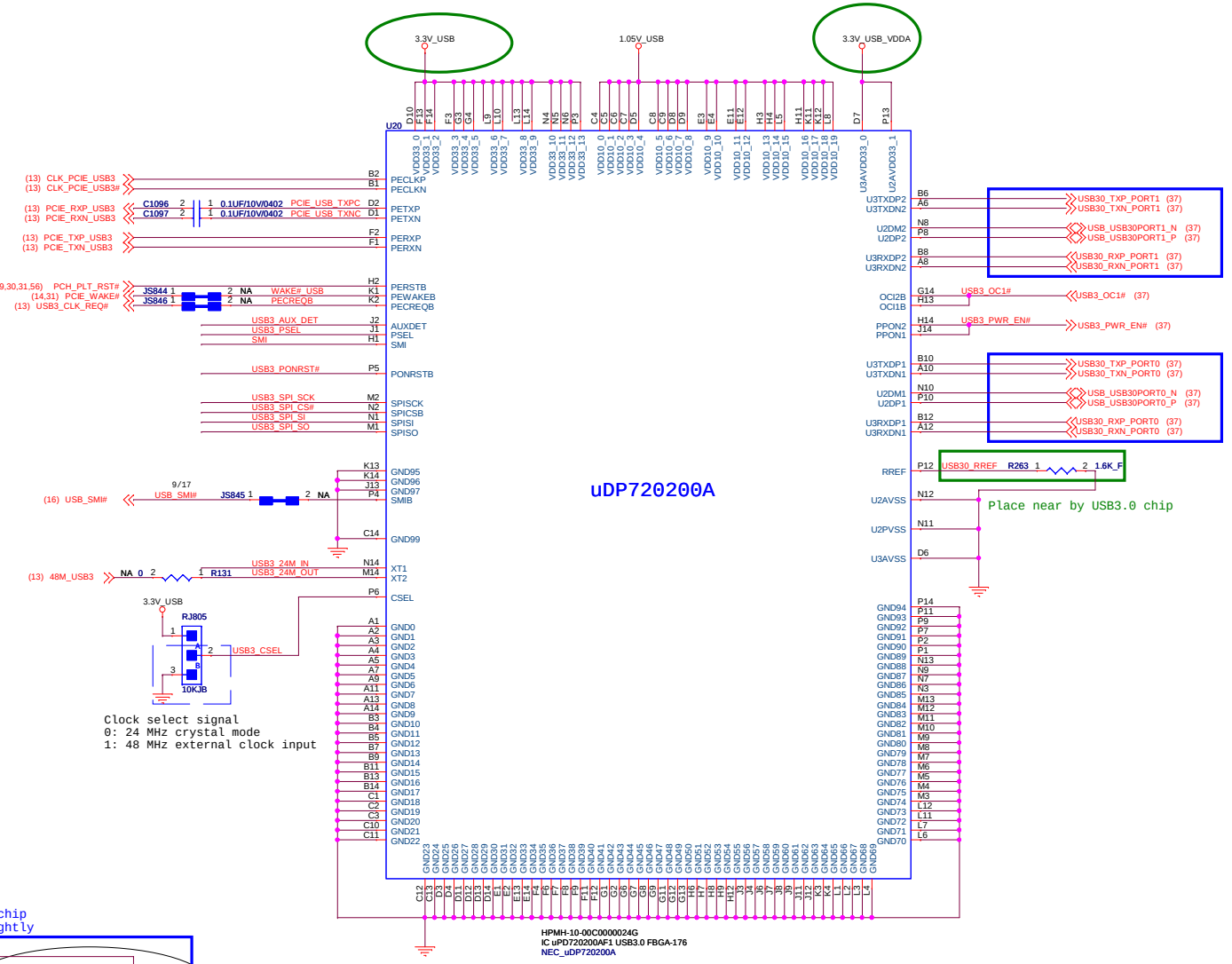












FLEX Computing			
Project Name : H710DI1	Title : USB30_uDP720200		
Size :	Document Number : HPMH-40GAB6600-B130	Rev : B	
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7/14

USB 2.0 NA
USB 3.0 Mount

Correvtive the ESD link topology. 20100810

USB2.0 CONN USE HPMH-38-0040000060G
USB3.0 CONN USE HPMH-38-0040000065G

USB 2.0 2nd Source
HPMH-38-0040000078G
HPMH-38-0040000080G
HPMH-38-0040000087G

USB 3.0 2nd Source
HPMH-38-0040000085G
HPMH-38-0040000068G
HPMH-38-0040000088G

USB 2.0 NA
USB 3.0 Mount

Correvtive the ESD link topology. 20100810

USB2.0 CONN Main Source HPMH-38-0040000066G
USB3.0 CONN Main Source HPMH-38-0040000065G

USB3.0 3.3V

500mW / 3.3V
(0.151Amp)

20100921

USB3.0 1.05V_USB

593mW / 1.05V
(0.72Amp)

Vout=0.8*(R1+R2)/R2

USB 2.0 Mount
USB 3.0 NA

USB2.0 MOUNTED
USB3.0 NA

USB2.0 MOUNTED
USB3.0 NA

USB POWER SW

2A

7/14 for USB3.0 and USB 2.0

7/14 USB 3.0 mount B
USB 2.0 mount B

Don't delete this pull-down resistor for disable Power SW in G3.

7/14 for USB3.0 (A)and USB 2.0(B)

Project Name : H710DI1	Title : USB30_CNN/PWR_SW/1.1V/3.3V
Size :	Document Number : HPMH-40GAB6600-B130 Rev : B
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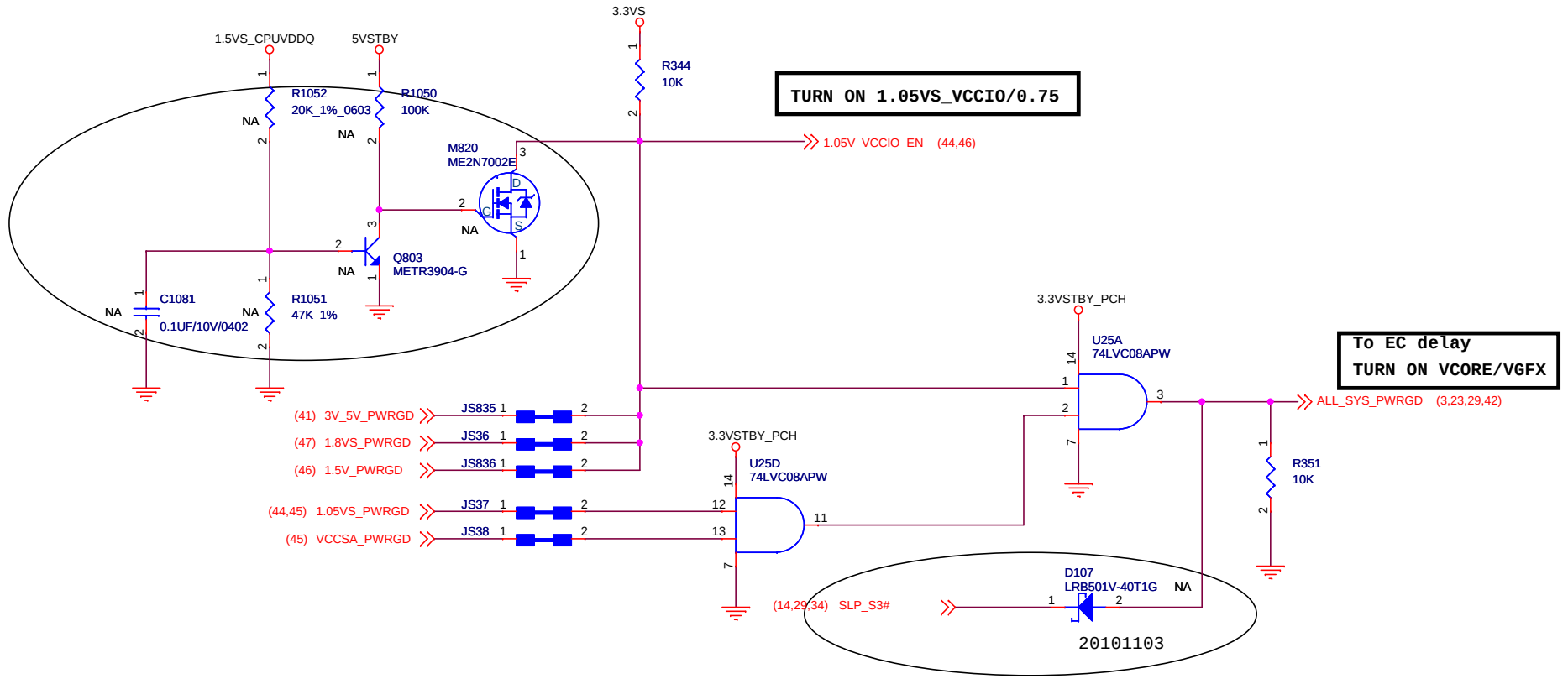
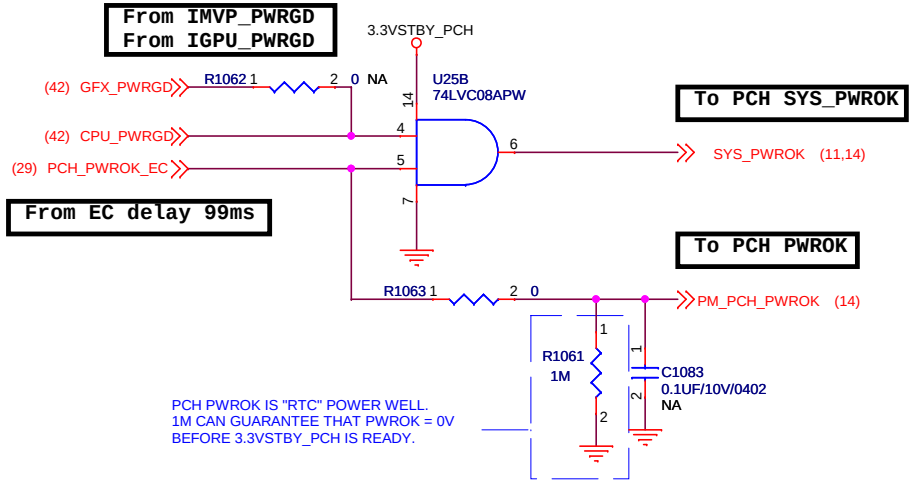
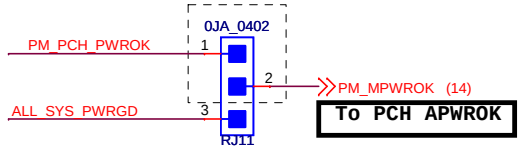
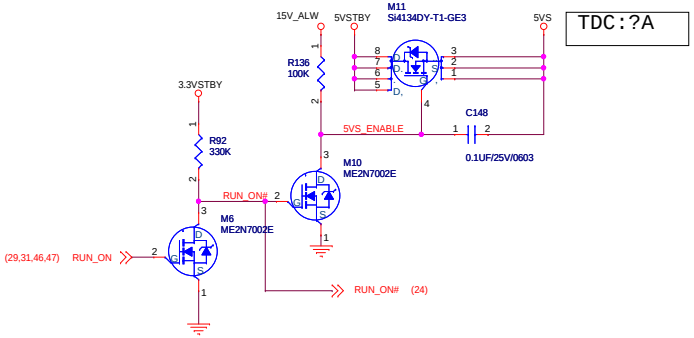




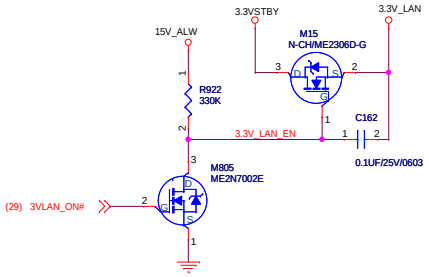


FLEX Computing

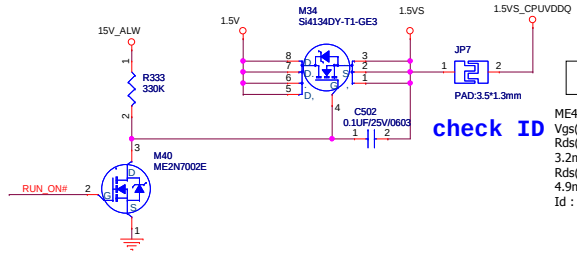
Project Name : H710DI1	Title : POWER_GOOD
Size : Custom	Document Number : HPMH-40GAB6600-B130
Rev : B	
Date: Monday, November 08, 2010	Sheet : 38 of 63



TDC:?A



TDC:0.3A

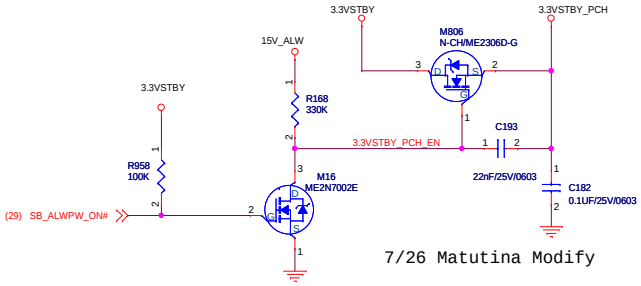


TDC:?A

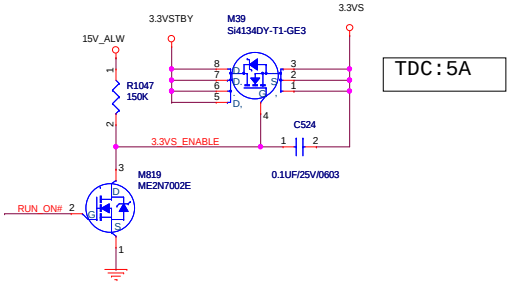
check ID

ME4626 :
Vgs(th): 3V(max)
Rds(on):
3.2m@Vgs = 10V (Max)
Rds(on):
4.9m@Vgs = 4.5V (Max)
Id : 23A

TDC:0.6A



7/26 Matutina Modify



TDC:5A

3.3V

ME2306D:

Vgs(th) : 1.0V(min),3.0V(max)
Rds(on) : 31m@Vgs = 10V(MAX)
Rds(on) : 52m@Vgs = 4.5V(MAX)
Id : 3.9A(Max)

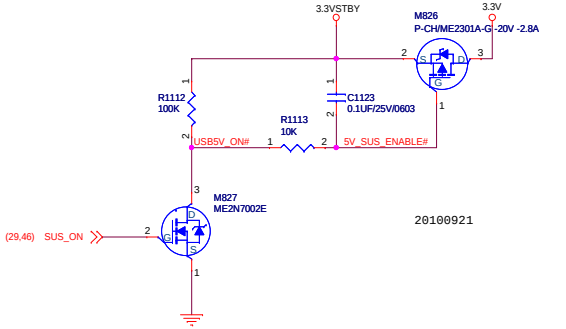
ME4894-G:

Vgs(th) : 1.0V(min),3.0V(max)
Rds(on) : 11.7m@Vgs = 10V (MAX)
Rds(on) : 18.2m@Vgs = 4.5V(MAX)
Id : 11.5A(Max)

ME2301A:

Vgs(th) : -0.9V(max)
Rds(on) : 75m@Vgs = -4.5V(MAX)
Id : -2.8A(Max)

500mW / 3.3V



20100921

FLEX Computing

Project Name : H710DI1	Title : RUN_PWR & SUS_PWR
Size : Custom	Document Number : HPMH-40GAB6600-B130
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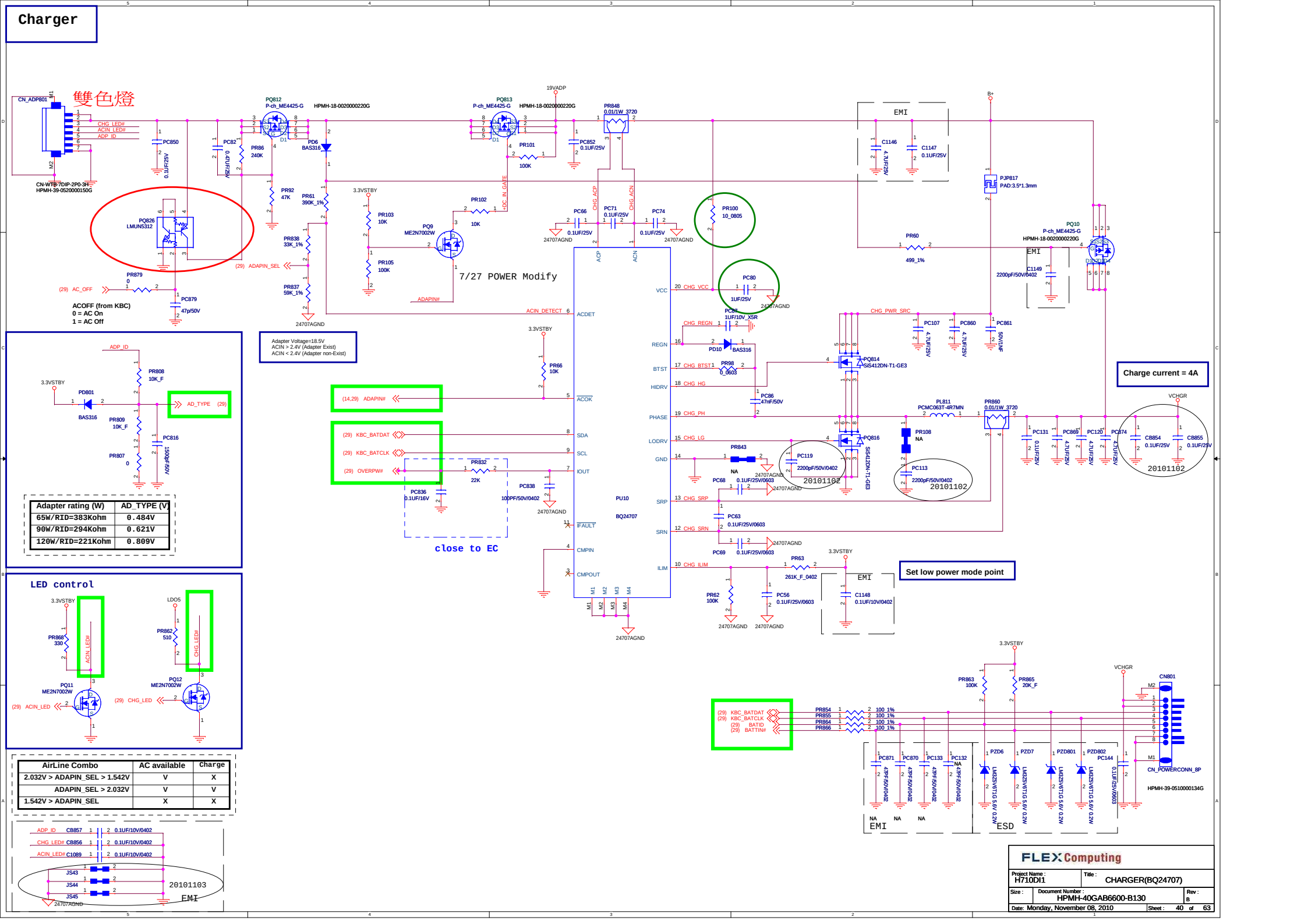
Charger


雙色燈
CN_ADP801
CN-WTB-7DIP-2P0-3H
HPMH-39-0520000150G
CHG_LED#
ACIN_LED#
ADP_ID
PQ826
LMUN5312
PQ812
P-ch_ME4425-G
HPMH-18-0020000220G
PQ813
PD6
BAS316
PR86
240K
PR92
47K
PR61
390K_1%
PR838
33K_1%
PR837
59K_1%
PR879
0
PC879
47pf/50V
(29) AC_OFF
(29) ADAPIN_SEL
ACOFF (from KBC)
0 = AC On
1 = AC Off
24707AGND
19VADP
PR848
0.01/1W_3720
PR101
100K
PC852
0.1UF/25V
3.3VSTBY
PR103
10K
PR105
100K
PR102
10K
PQ9
ME2N7002W
PC66
PC71
PC74
0.1UF/25V
CHG_ACP
CHG_ACN
DC_IN_GATE
ADAPIN#
7/27 POWER Modify
PR100
10_0805
PC80
1UF/25V
PC81
1UF/10V_X5R
ACIN_DETECT
ACDET
ACOK
SDA
SCL
IOUT
IFAULT
CMPIN
CMPOUT
PU10
BQ24707
VCC
REGN
BTST
HIDRV
PHASE
LODRV
GND
SRP
SRN
ILIM
CHG_VCC
CHG_REGN
CHG_BTST
CHG_HG
CHG_PH
CHG_LG
CHG_SRP
CHG_SRN
CHG_ILIM
PD10
PR98
0_0603
PC86
47nF/50V
PR843
NA
PC68
PC69
PC63
PC56
0.1UF/25V/0603
PR62
100K
PR63
261K_F_0402
C1148
0.1UF/10V/0402
EMI
B+
PJP817
PAD:3.5*1.3mm
C1146
4.7UF/25V
C1147
0.1UF/25V
PR60
499_1%
PQ10
P-ch_ME4425-G
HPMH-18-0020000220G
C1149
2200pF/50V/0402
CHG_PWR_SRC
PC107
PC860
4.7UF/25V
PC861
50V/1NF
PQ814
SIS412DN-T1-GE3
PQ816
SIS412DN-T1-GE3
PL811
PCMC063T-4R7MN
PR860
0.01/1W_3720
PR108
NA
PC119
2200pF/50V/0402
20101102
PC113
2200pF/50V/0402
20101102
PC131
PC865
PC120
PC874
0.1UF/25V
4.7UF/25V
CB854
CB855
VCHGR
Charge current = 4A
Set low power mode point
(14,29) ADAPIN#
(29) KBC_BATDAT
(29) KBC_BATCLK
(29) OVERPW#
PR832
22K
PC836
0.1UF/16V
PC838
100PF/50V/0402
close to EC
ADP_ID
PR808
10K_F
PD801
BAS316
PR809
10K_F
PR807
0
PC816
(29) AD_TYPE
Adapter rating (W) | AD_TYPE (V)
65W/RID=383Kohm | 0.484V
90W/RID=294Kohm | 0.621V
120W/RID=221Kohm | 0.809V
Adapter Voltage=18.5V
ACIN > 2.4V (Adapter Exist)
ACIN < 2.4V (Adapter non-Exist)
LED control
PR868
330
PQ11
ME2N7002W
(29) ACIN_LED
LDO5
PR862
510
PQ12
ME2N7002W
(29) CHG_LED
AirLine Combo | AC available | Charge
2.032V > ADAPIN_SEL > 1.542V | V | X
ADAPIN_SEL > 2.032V | V | V
1.542V > ADAPIN_SEL | X | X
CB857
CB856
C1089
0.1UF/10V/0402
JS43
JS44
JS45
20101103
EMI
(29) KBC_BATDAT
(29) KBC_BATCLK
(29) BATID
(29) BATTIN#
PR854
PR855
PR864
PR866
100_1%
PR863
100K
PR865
20K_F
CN801
CN_POWERCONN_8P
HPMH-39-0510000134G
PC871
PC870
PC133
PC132
47PF/50V/0402
PZD6
PZD7
PZD801
PZD802
LMZ25V6T1G 5.6V 0.2W
PC144
0.1UF/25V/0603
ESD
NA
EMI
FLEX Computing
Project Name : H710DI1
Title : CHARGER(BQ24707)
Size :
Document Number : HPMH-40GAB6600-B130
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5V / 3.3VSTBY

Freq=300KHz
TDC = 7 A
OCP = 10 A

Freq=375KHz
TDC = 4 A
OCP = 5.7A

PU9
TPS51125RGER

5V/3.3VSTBY ON

TRIP 3V

TRIP 5V

Current limit

ENTrip floating active

* Options 1.
5VSTBY

* Options 2.

* Options 3.
(38) 3V_5V_PWRGD

Vo=(1+R1/R2)*2
(1+32.4K/21K)*2= 5..08V

Vo=(1+R1/R2)*2
= (1+13/20)*2 = 3.3V

For RT8205A
PR92 must MOUNTED
PR94 must NA

INTEL HR / AMD DANUBE
Options 1 - 5VSTBY / 5V
Options 2 - 5VALW_ON / SUS_ON
Options 3 - 3V_5V_PWRGD / 3.3V_5V_PWRGD
Options 4 - 15V_ALW / 15VSTBY
Options 5 - 5VSTBY / 5V

VREG5 : 5V -> 365KHz , 3.3V -> 460KHz
VREG3: 5V -> 300KHz , 3.3V -> 375KHz

7/28 power Modify

For PCB Acustic Noise

PU3-m1
For layout request, no connect anything.

+15V Charge pump

Table 3. Enabling State

EN0	ENTRIP1	ENTRIP2	VREF	VREG5	VREG3	CH1	CH2	VCLK
GND	Don't Care	Don't Care	Off	Off	Off	Off	Off	Off
R to GND	Off	Off	On	On	On	Off	Off	Off
R to GND	On	Off	On	On	On	On	Off	Off
R to GND	Off	On	On	On	On	Off	On	Off
R to GND	On	On	On	On	On	On	On	Off
Open	Off	Off	On	On	On	Off	Off	Off
Open	On	Off	On	On	On	On	Off	On
Open	Off	On	On	On	On	Off	On	Off
Open	On	On	On	On	On	On	On	On

FLEX Computing

Project Name : H710DI1	Title : 5VSTBY_3VSTBY(TPS51125)
Size : Custom	Document Number : HPMH-40GAB6600-B130 Rev : B
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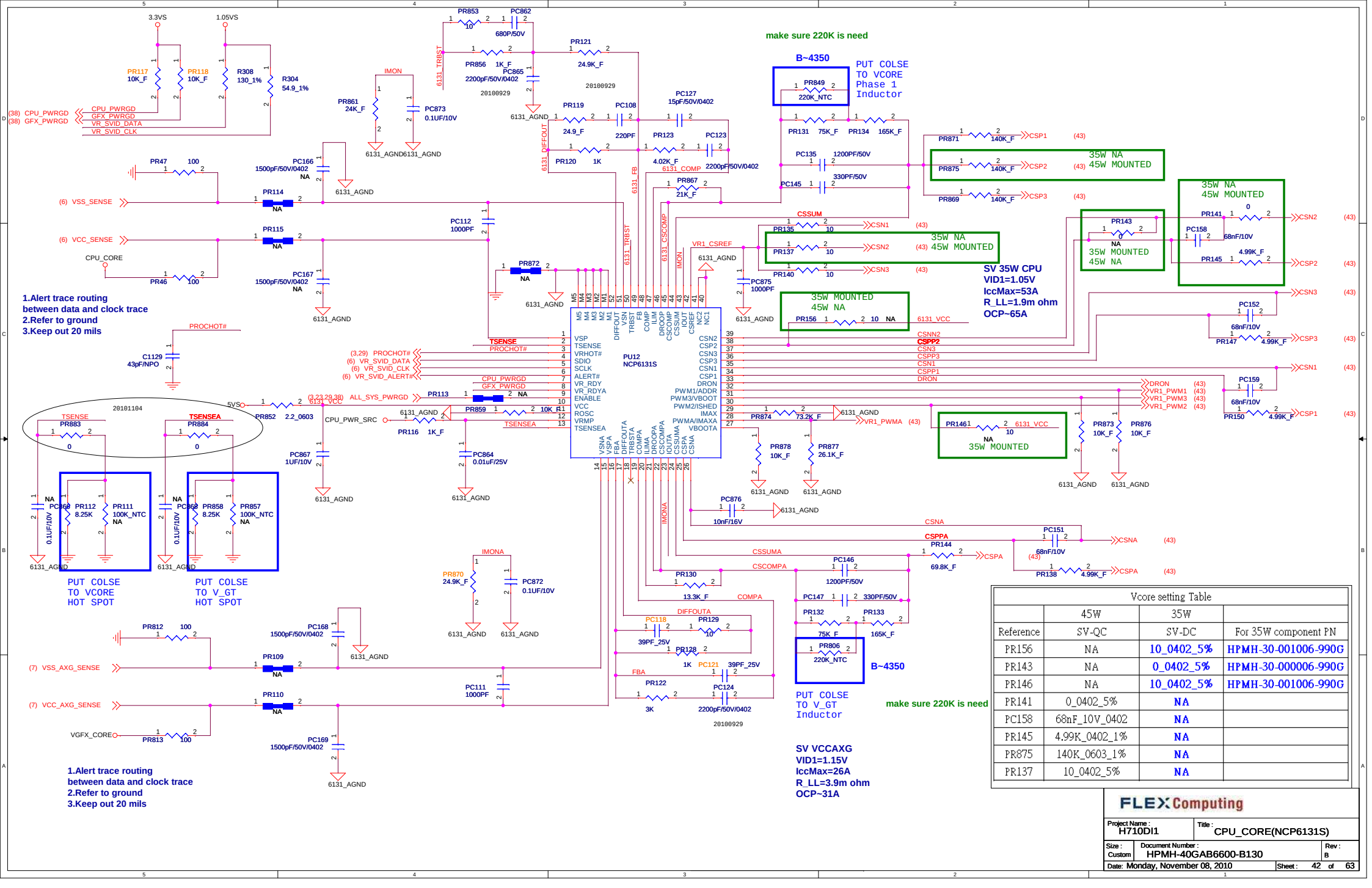

Vcore setting Table			
	45W	35W	
Reference	SV-QC	SV-DC	For 35W component PN
PR156	NA	10_0402_5%	HPMH-30-001006-990G
PR143	NA	0_0402_5%	HPMH-30-000006-990G
PR146	NA	10_0402_5%	HPMH-30-001006-990G
PR141	0_0402_5%	NA	
PC158	68nF_10V_0402	NA	
PR145	4.99K_0402_1%	NA	
PR875	140K_0603_1%	NA	
PR137	10_0402_5%	NA	

FLEX Computing

Project Name : H710DI1	Title : CPU_CORE(NCP6131S)	
Size : Custom	Document Number : HPMH-40GAB6600-B130	Rev : B
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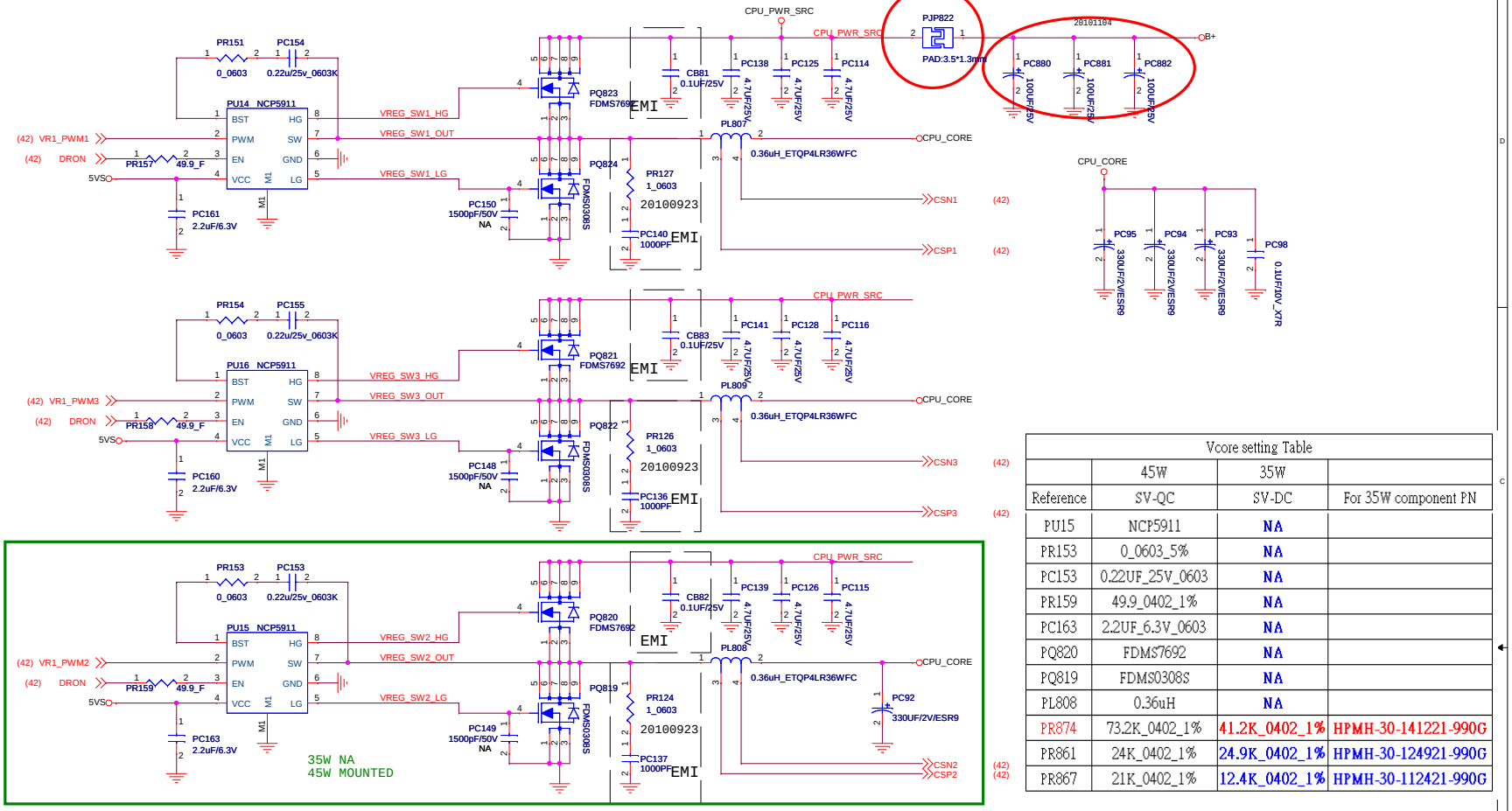

Vcore setting Table			
	45W	35W	
Reference	SV-QC	SV-DC	For 35W component PN
PU15	NCP5911	NA	
PR153	0_0603_5%	NA	
PC153	0.22UF_25V_0603	NA	
PR159	49.9_0402_1%	NA	
PC163	2.2UF_6.3V_0603	NA	
PQ820	FDMS7692	NA	
PQ819	FDMS0308S	NA	
PL808	0.36uH	NA	
PR874	73.2K_0402_1%	41.2K_0402_1%	HPMH-30-141221-990G
PR861	24K_0402_1%	24.9K_0402_1%	HPMH-30-124921-990G
PR867	21K_0402_1%	12.4K_0402_1%	HPMH-30-112421-990G

FLEX Computing

Project Name : H710DI1	Title : CPU_CORE_DRIVER(NCP5911)
Size :	Document Number : HPMH-40GAB6600-B130 Rev : B
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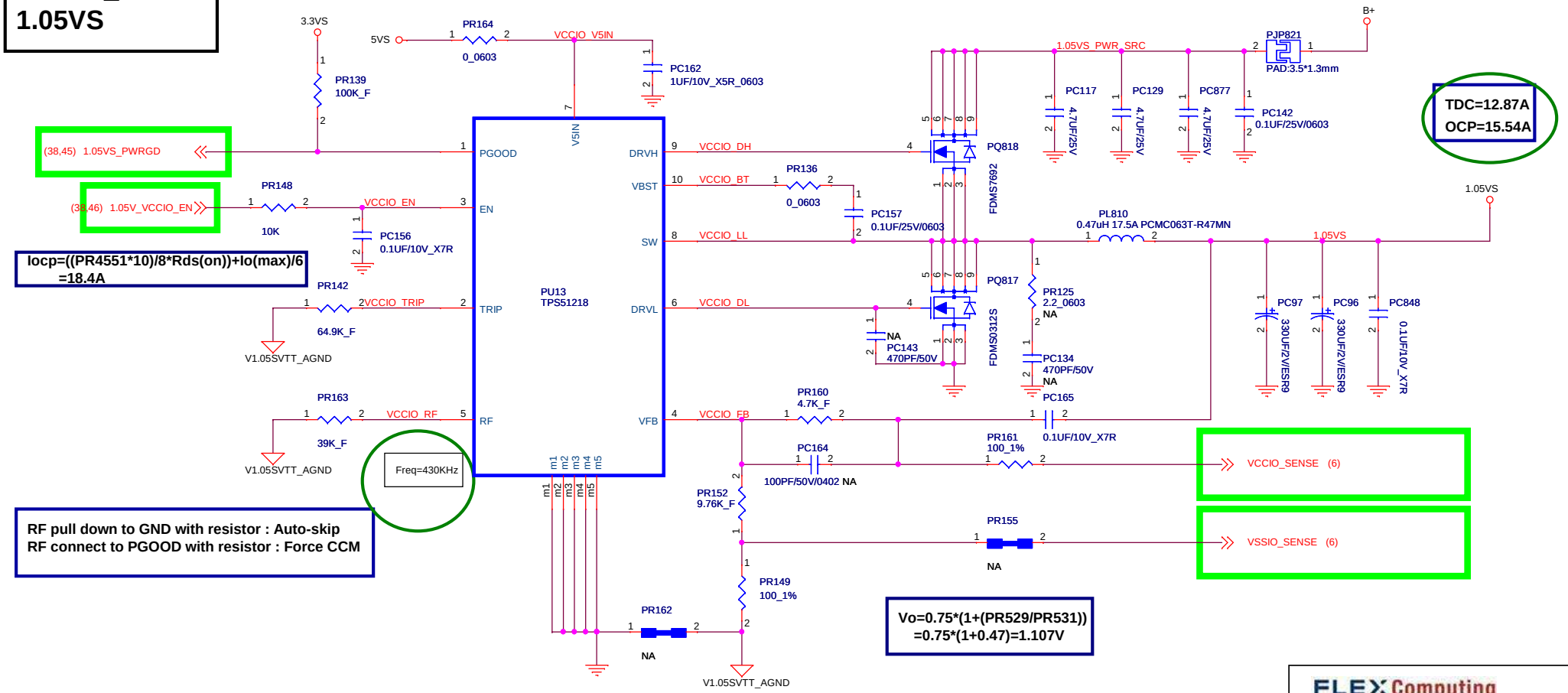
1.05VS_VCCIO
1.05VS



FLEX Computing

Project Name : H710DI1	Title : 1.05VS(TPS51218)
Size : Custom	Document Number : HPMH-40GAB6600-B130
Rev : B	
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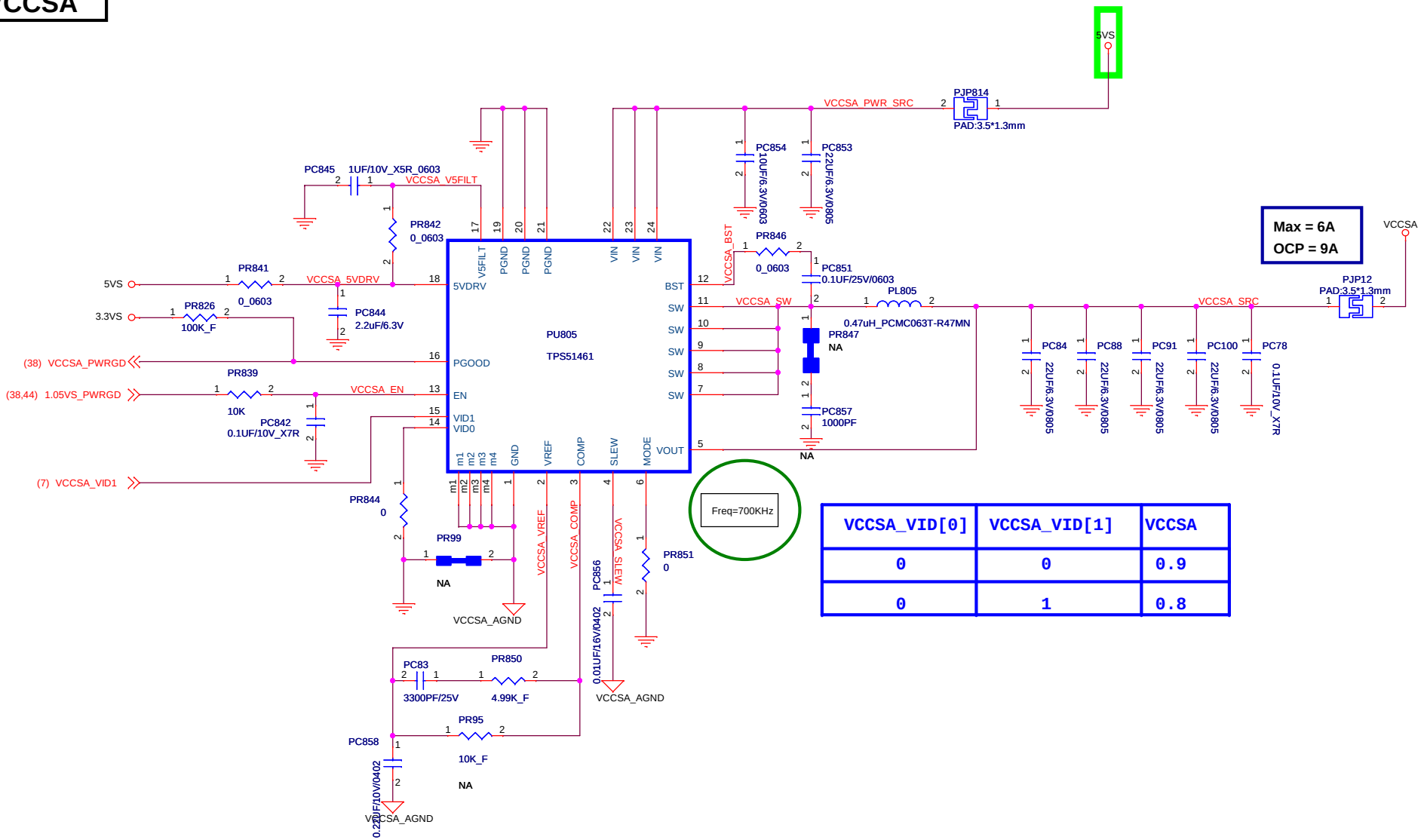
VCCSA



VCCSA_VID[0]	VCCSA_VID[1]	VCCSA
0	0	0.9
0	1	0.8

FLEXComputing

Project Name : H710DI1	Title : ITE8509E/ 1.1VS	
Size : B	Document Number : HPMH-40GAB6600-B130	Rev : B
Date: Monday, November 08, 2010	Sheet : 45 of 63	

1.5V

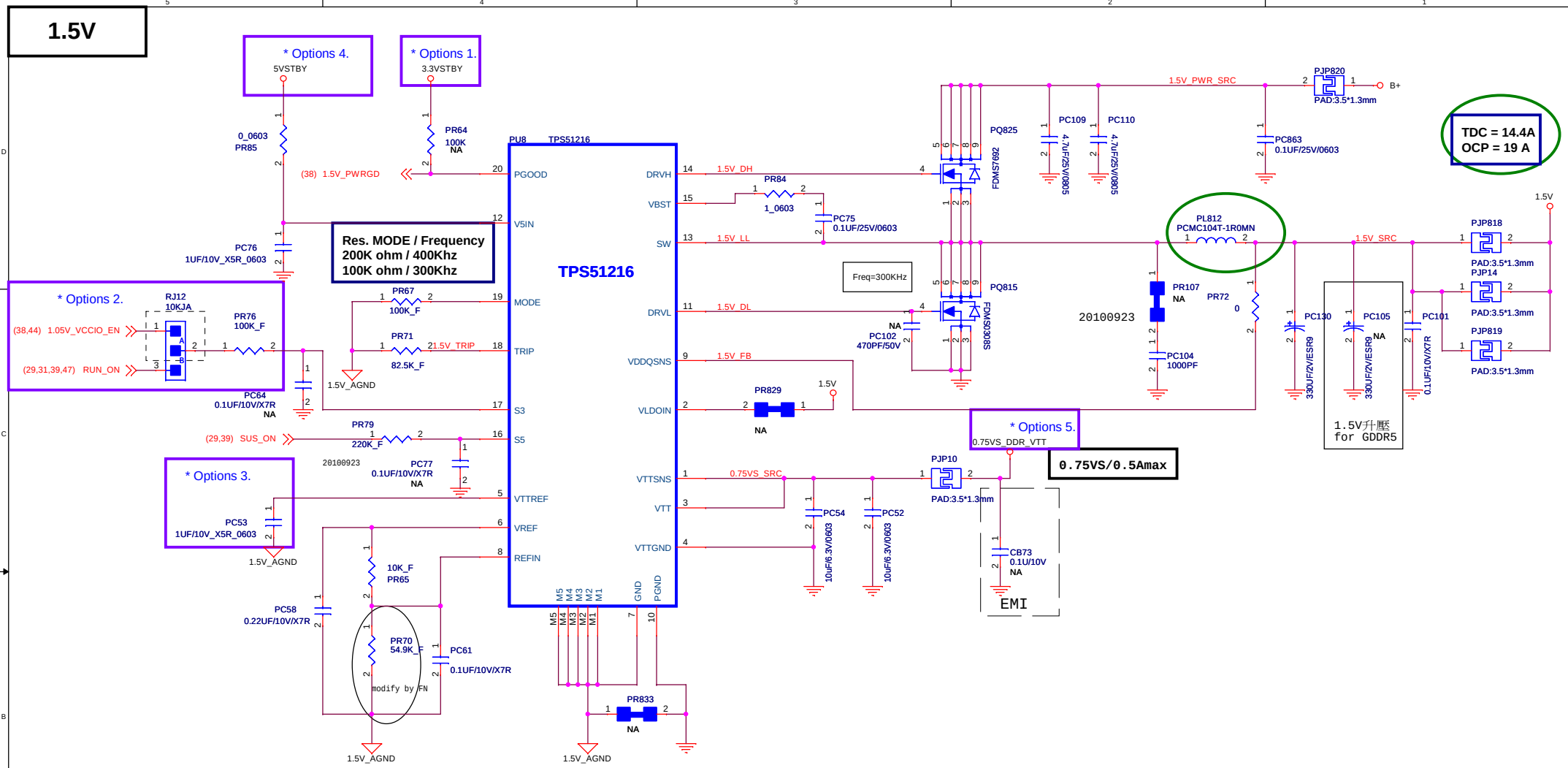


Table 1. S3 and S5 Control Table

STATE	S3	S5	VTTREF	VTT
S0	H	H	1	1
S3	L	H	1	0 (high-Z)
S4/S5	L	L	0 (discharge)	0 (discharge)

INTEL HR / AMD DANUBE

Options 1 - 3.3VSTBY / 3.3V

Options 2 - RUN_ON / SUS_ON

Options 3 - DDR_VTTR / V_DDR_VTT

Options 4 - 5VSTBY / 5V

Options 5 - 0.75VS_DDR_VTT / 0.75V_DDR_VTT

FLEXComputing

Project Name : H710DI1	Title : DDR_PWR(TPS51216)
Size :	Document Number : HPMH-40GAB6600-B130 Rev : B
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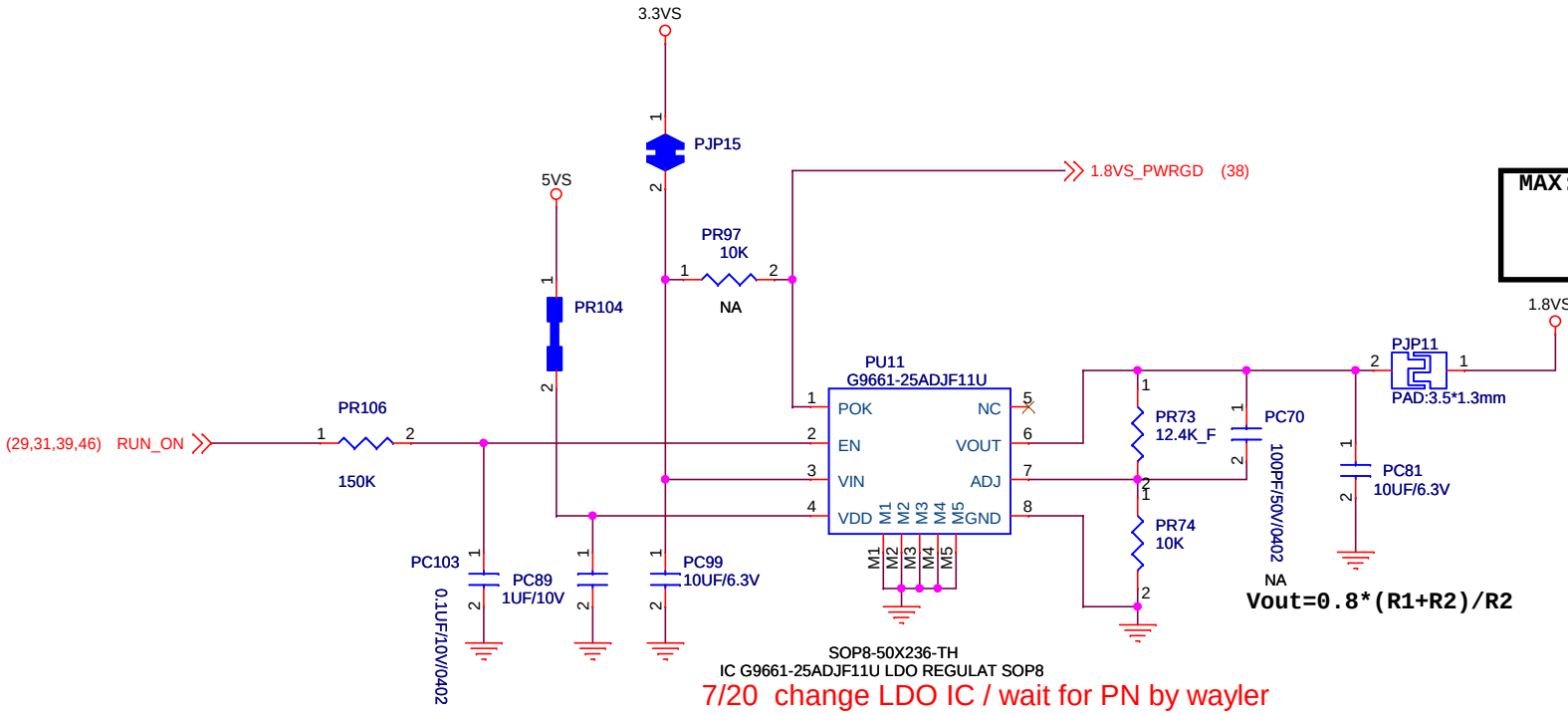
1.8VS



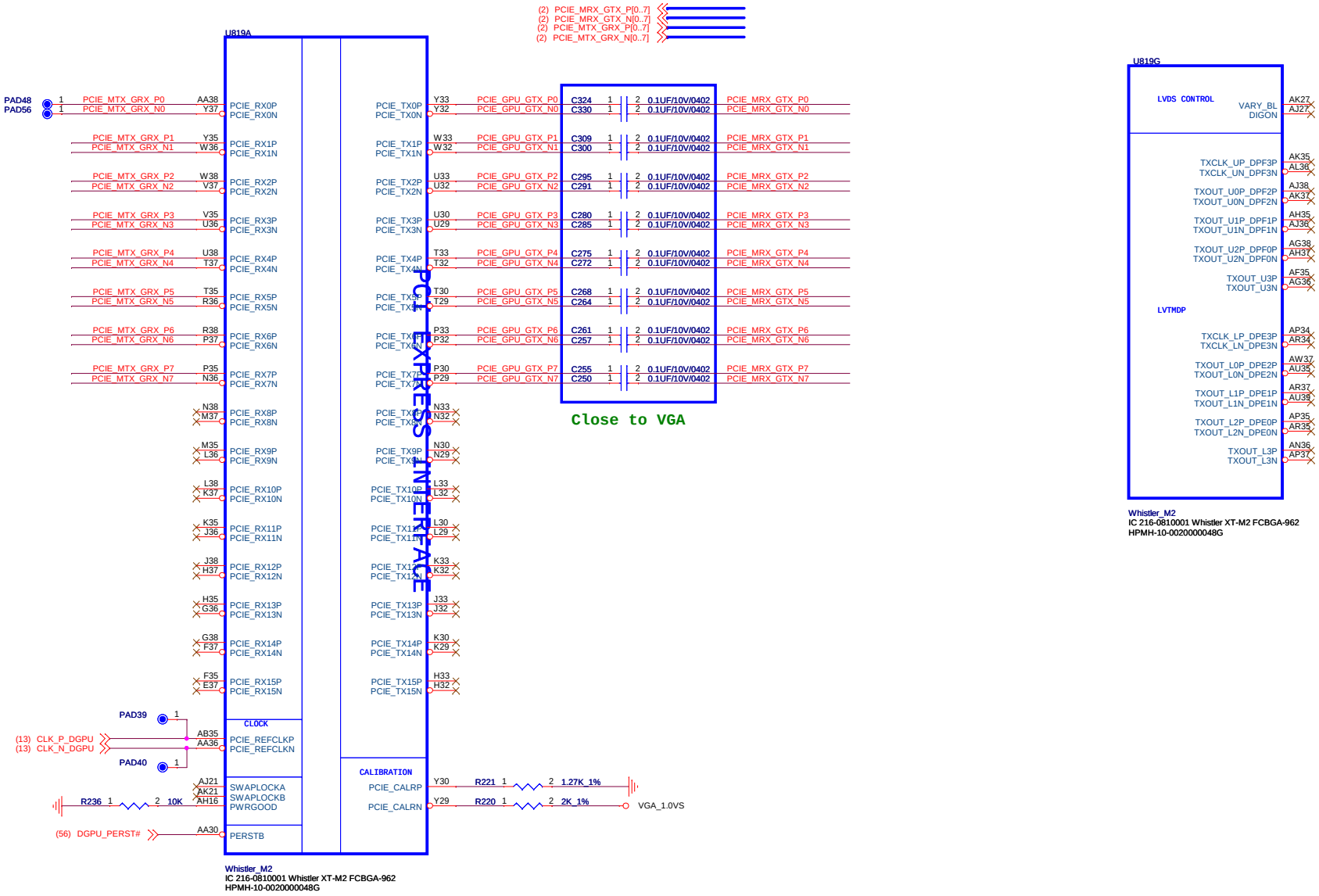
MAX:
UI=1.45A

1.8VS for CPU & PCH

7/20 change LDO IC / wait for PN by wayler

FLEX Computing

Project Name : H710DI1	Title : 1.8VS	
Size :	Document Number : HPMH-40GAB6600-B130	Rev : B
Date: Monday, November 08, 2010	Sheet : 47 of 63	



GPU TYPE	PN
Whistler XT	HPMH-10-0020000048G
Seymour-XT	HPMH-10-0020000049G

FLEX Computing

Project Name : H710DI1	Title : Capilano_1/5_PCIE/LVDS
Size :	Document Number : HPMH-40GAB6600-B130 / Rev : B
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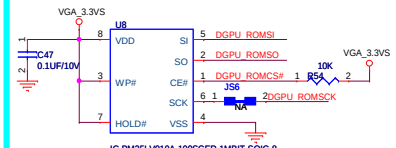
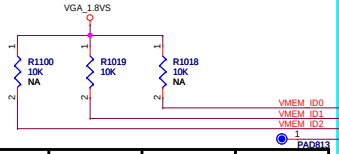
For del vBIOS ROM design:
1.P49 -U8,C47,R54
2.P53 -R1001,R1002,R1015

For GDDR5 used



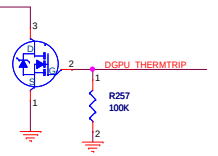
NA for del vBIOS ROM design.

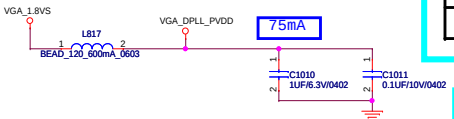
VMEM_ID

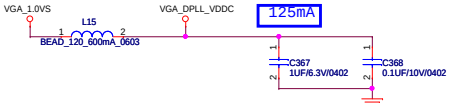


	DVPDATA_2	DVPDATA_1	DVPDATA_0
Seymour Hynix H5GQ2H24MFR-T2C (128Mx16) x4pcs	0	0	0
Seymour Samsung K4G20325FC-HC04 (128Mx16) x4pcs	0	0	1
Whistler Hynix H5GQ1H24AFR-T2C (64Mx16) x8pcs	0	1	0
Whistler Samsung K4G10325FE-HC04 (64Mx16) x8pcs	0	1	1
Seymour Hynix H5GQ1H24AFR-T2C (64Mx16) x4pcs	1	0	0
Seymour Samsung K4G10325FE-HC04 (64Mx16) x4pcs	1	0	1
Seymour Elpida EDW2032BABG-50-F(128Mx16) x4pcs	1	0	1
Whistler Elpida EDW1032BABG-50-F(64Mx16) x8pcs	1	1	1

OD, PU is at PWRGD circuit

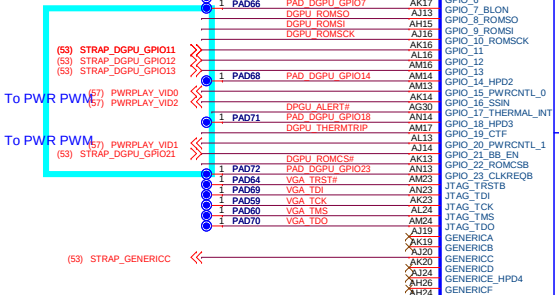


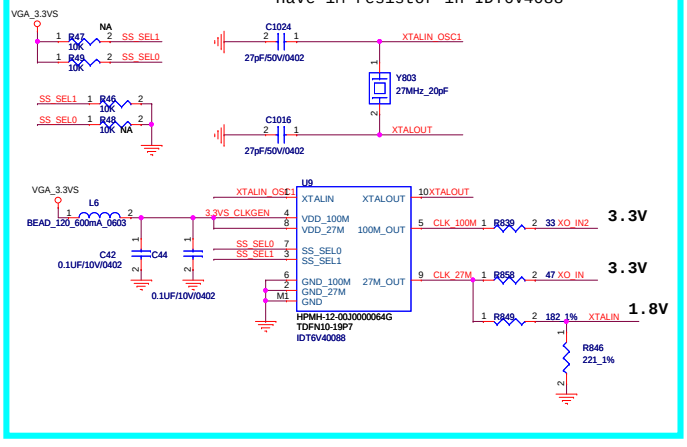


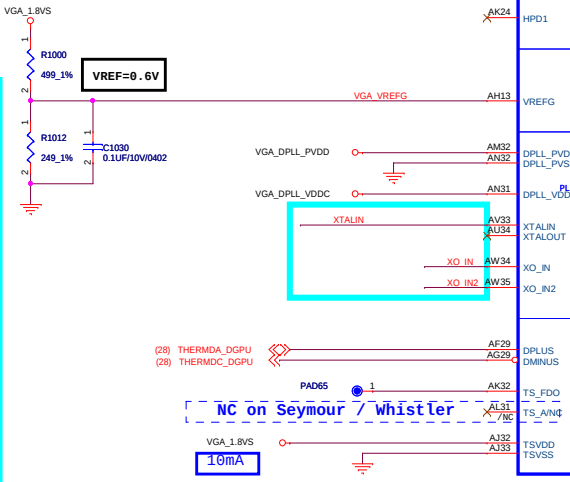


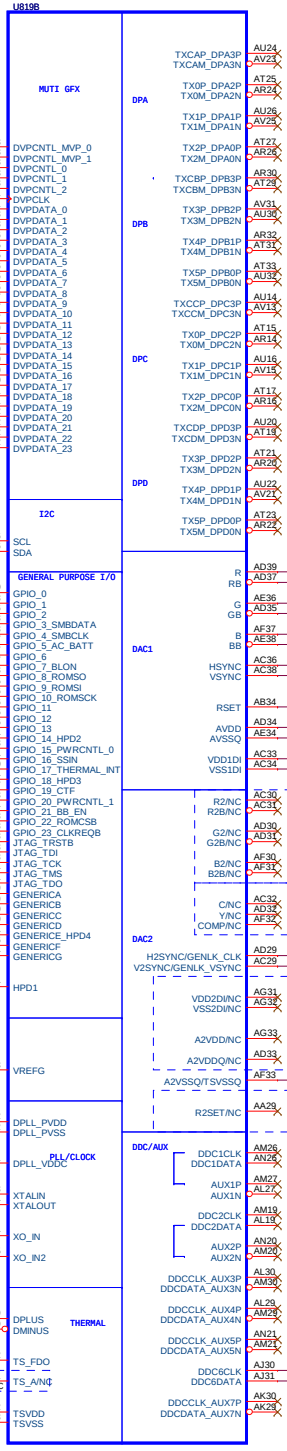
100 MHz Spread Selection Table

PIN3	PIN7	PIN5	
S1	S0	Down Spread%	
L	L	OFF	
L	M	-0.5	
L	H	-2.5	
M	L	-0.25	
M	M	-0.75	
M	H	-1.0	
H	L	-1.5	
H	M	-2.0	Default
H	H	-3.0	

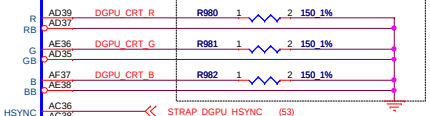








For DGPU debug, mounted Close to chipset



NC on Seymour / Whistler

For DGPU debug

FLEXComputing			
Project Name : H710DI1		Title : Capilano_2/5_DP/DAC/GPIO	
Size :	Document Number : HPMH-40GAB6600-B130		Rev : B
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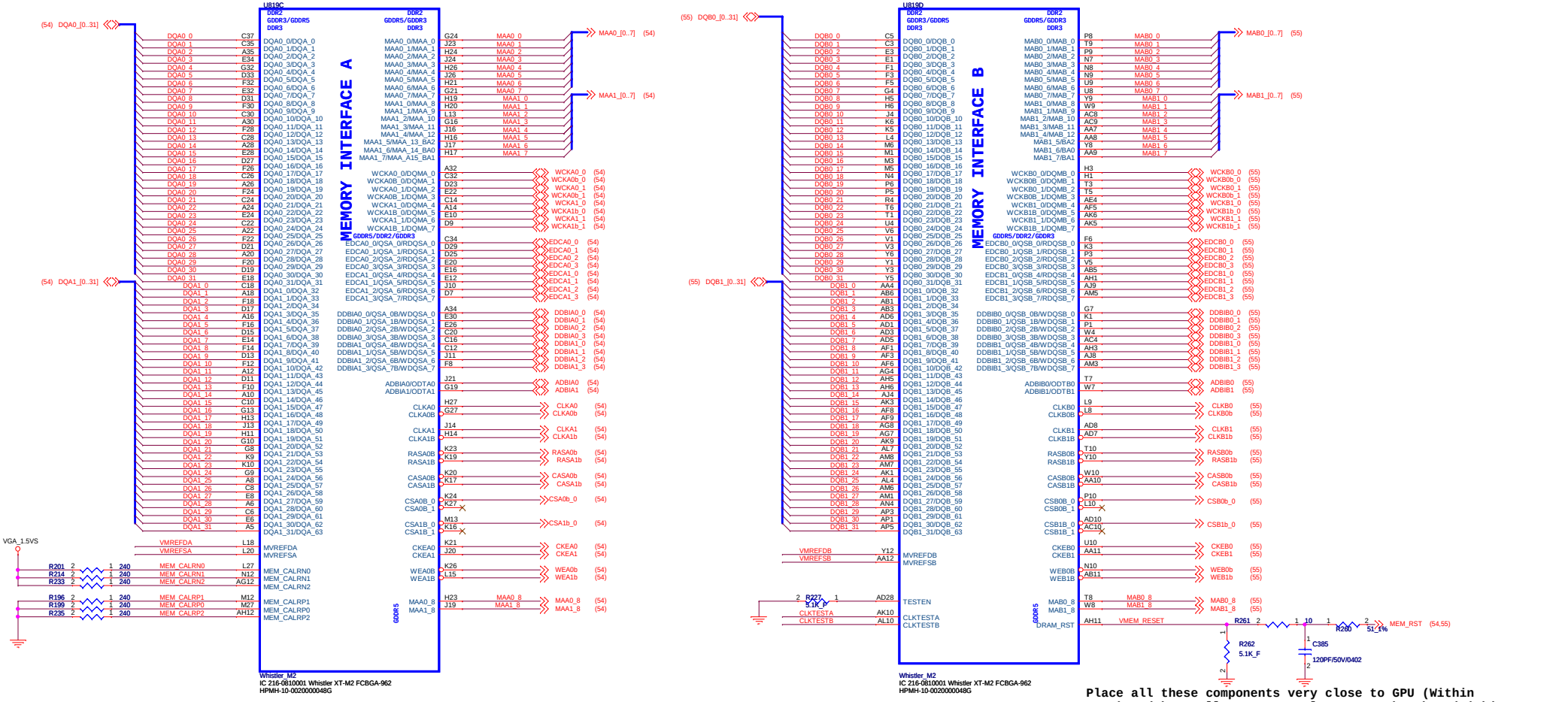
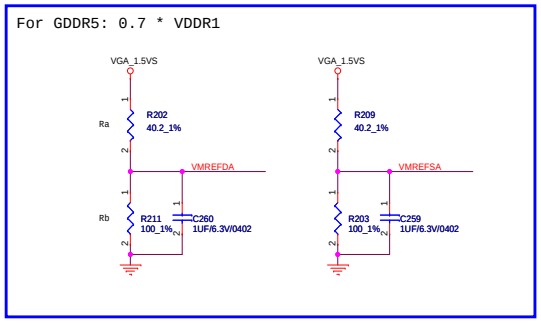
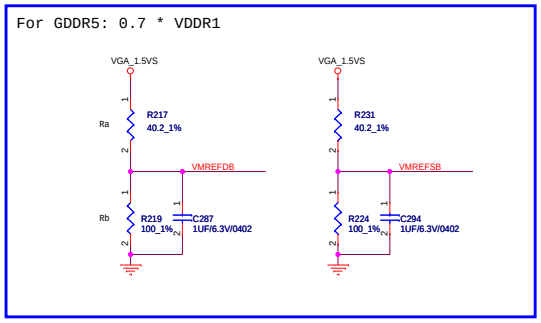
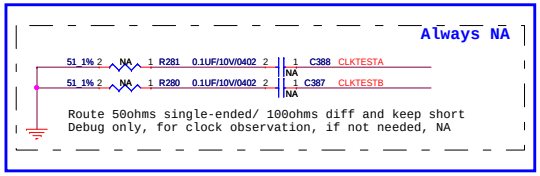


Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

VRAM TYPE		PN
Hynix H5GQ1H24AFR-T2C	64MX16(32MX32)	HPMH-14-0030000001G
Hynix H5GQ2H24MFR-T2C	128MX16(64MX32)	HPMH-14-0030000002G
SAMSUNG K4G10325FE-HC04	64MX16(32MX32)	HPMH-14-0030000003G
SAMSUNG K4G20325FC-HC04	128MX16(64MX32)	HPMH-14-0030000004G
Elpida EDW1032BABG-50-F	64MX16(32MX32)	HPMH-14-0030000005G
Elpida EDW2032BABG-50-F	128MX16(64MX32)	HPMH-14-0030000006G

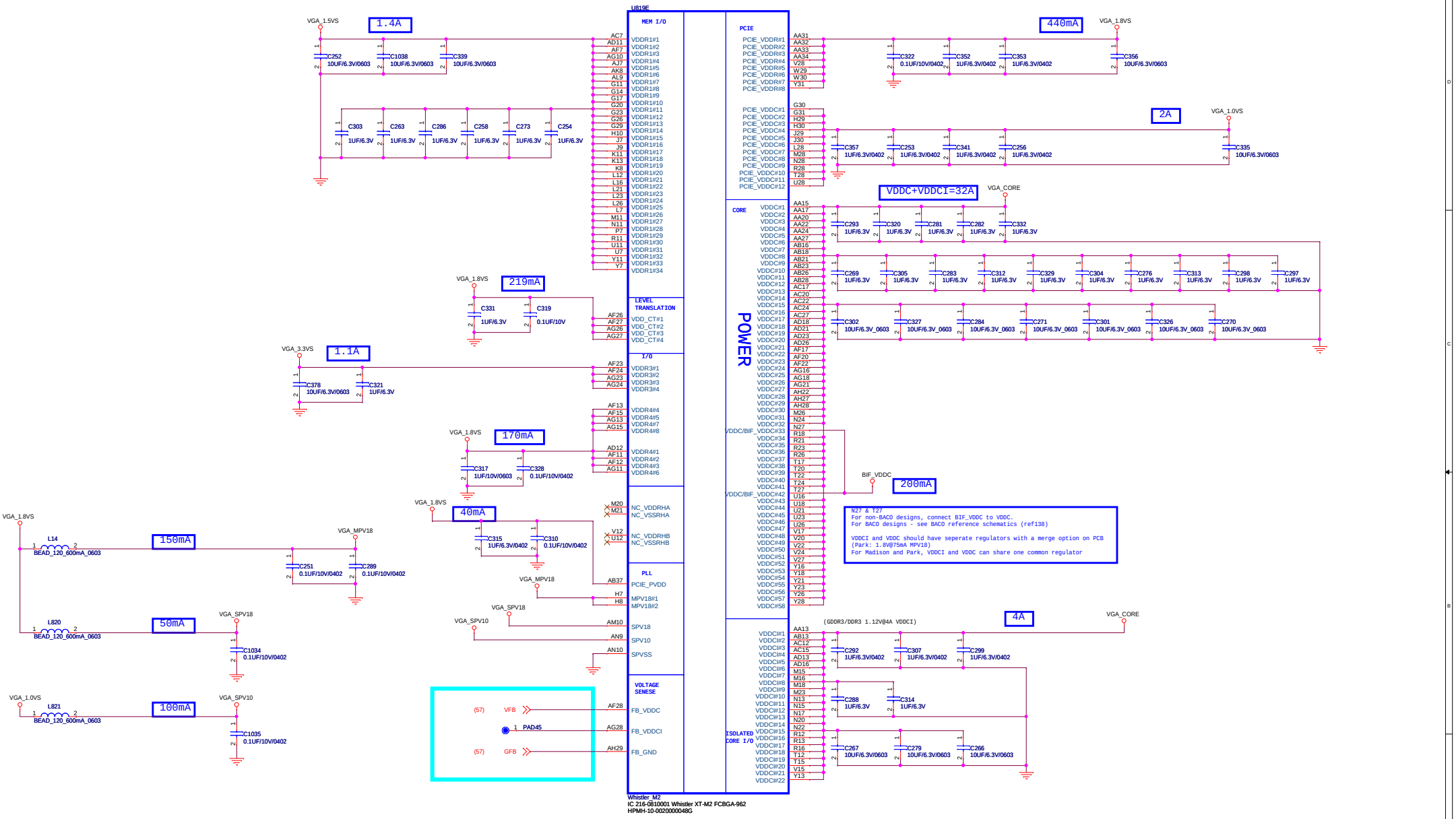




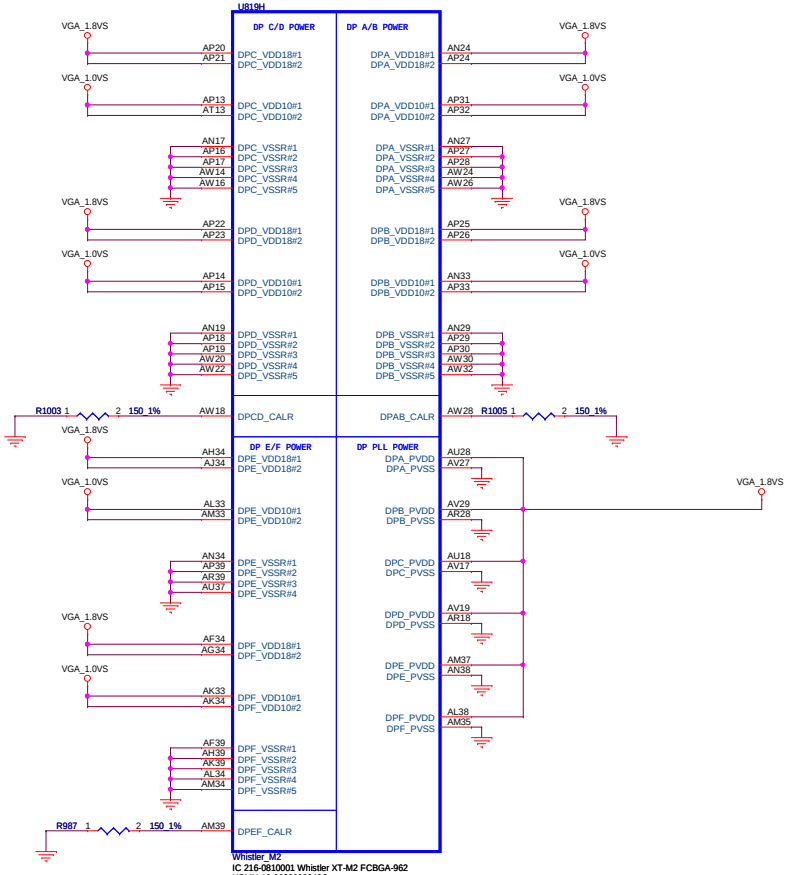


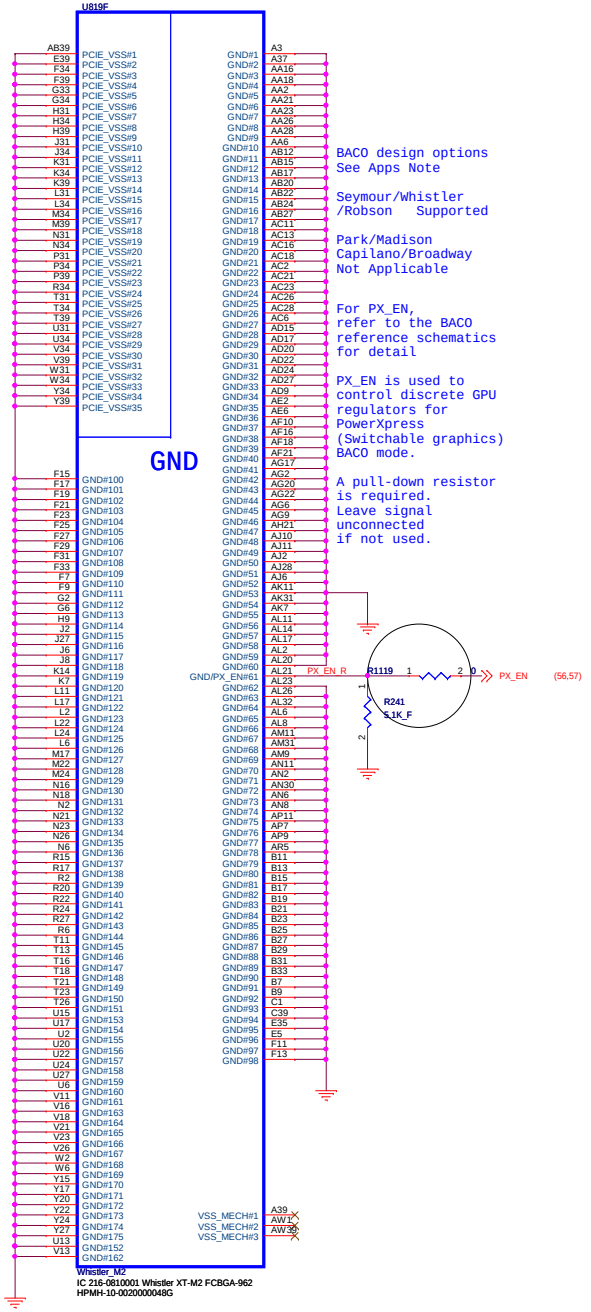
FLEX Computing

Project Name : H710DI1	Title : Capilano_3/5_VRAM_ IF	
Size :	Document Number : HPMH-40GAB6600-B130	Rev : B
Date: Monday, November 08, 2010	Sheet : 50 of 63	



FLEXComputing			
Project Name : H710DI1	Title : Capilano_4/5_PWR_IO		
Size :	Document Number : HPMH-40GAB6600-B130	Rev : B	
Date: Monday, November 08, 2010	Sheet : 51 of 63		





BACO design options
See Apps Note

Seymour/Whistler
/Robson Supported

Park/Madison
Capilano/Broadway
Not Applicable

For PX_EN,
refer to the BACO
reference schematics
for detail

PX_EN is used to
control discrete GPU
regulators for
PowerXpress
(Switchable graphics)
BACO mode.

A pull-down resistor
is required.
Leave signal
unconnected
if not used.

FLEXComputing

Project Name : H710DI1	Title : Capilano_5/5_PWR_DAC/GND
Size :	Document Number : HPMH-40GAB6600-B130 Rev : B
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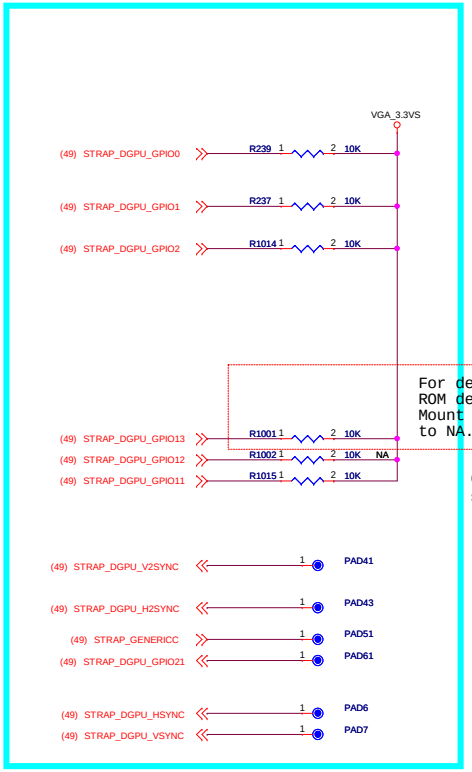
Signal	Seymour/Whistler	Robson/Park Medison/Capilano Broadway
Ball AC32 on M2	NC	DAC2 Output-C on M2 package
Ball AA29 on M2	NC	R2SET on M2 package
Ball AD32 on M2	NC	DAC2 Output- Y
Ball AG33 on M2	NC	A2VDD
Ball AD33 on M2	NC	A2VDDQ
Ball AF33 on M2	TSVSSQ	A2VSSQ
Ball AG33 AG32 on M2	NC	VDD2DI/VSS2DI
H2SYNC	GENLK_CLK: (3.3V) Reference clock input (3.3V) for pixel PLL received from frame-lock/ gen-lock interface	H2SYNC
V2SYNC	GENLK_VSYNC (3.3V) Frame timing indicator.Output to frame-lock/genlock interface	V2SYNC

Signal	Seymour/Whistler	Robson/Park Medison/Capilano Broadway
Ball AJ21 on M2 Ball AG13 on S3	SWAPLOCKA SwaplockA/B signals can be optionally used on a multi-GPU design with multiple display outputs to allow all displays in a group (group A or group B) to update at the same time and have synchronous left/right stereo timing. Genlock of the GPUs is also needed, either via a genlock system, or by feeding all GPUs with the same reference clock. Also connecting SwaplockB is preferred, but not required. SwaplockA/B are open drain, 3.3V signals. If this feature is not required, these signals can be used as 3.3V GPIOs or left unconnected on the PCB.	Ball AJ21 is NC on M2 packages Ball AG13 is R2SET on S3 package
Ball AK21 on M2 Ball H12 on S3	SWAPLOCKB – see above On a multi-gpu design,SwaplockB from all GPUs are connected together with an external pull-up resistor (10K Ohms). If this feature is not required, these signals can be used as 3.3V GPIOs or left unconnected on the PCB.	Ball AK21 is NC on M2 packages Ball AH12 is DAC2 Output- on S3 package

CONFIGURATION STRAPS

STRAPS	PIN	DESCRIPTION	ASIC Deault	Status
TX_PWRS_ENB	GPIO0	Transmitter (Tx) power savings enable. 0: 50% Tx output swing 1: Full Tx output swing (DEFAULT)	0 Internal Pull Down	Mounted
TX_DEEMPH_EN	GPIO1	PCI Express transmitter deemphasis enable. 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled (DEFAULT)		Mounted
RESERVED	GPIO2	0 : PCIe device as 2.5 GT/s capable 1 : PCIe device as 5.0 GT/s capable (DEFAULT)		Mounted
VGA_DIS	GPIO9	VGA disable determines whether or not the card will be recognized as the system's VGA controller (via the SUBCLASS field in the PCI configuration space): 0 : VGA Controller capacity enabled (DEFAULT) 1 : The device will not be recognized as the system's VGA controller		NA NA
BIOS_ROM_EN	GPIO_22_ROMCSB	Enable the external BIOS ROM device: 0 - Disable external BIOS ROM device (DEFAULT) 1 - Enable external BIOS ROM device		Mounted
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13 GPIO12 GPIO11	BIOS_ROM_EN = 1, Config[2:0] defines the ROM type. BIOS_ROM_EN = 0, Config[2:0] defines the primary memory aperture size Size of the primary memory apertures CONFIG[2:0] 128 MB 000 256 MB 001 (DEFAULT) 64 MB 010 32 MB 011		Mounted NA Mounted
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS L: Ignore VIP Device Strap (DEFAULT) H: Enable VIP Device Strap		NA
RESERVED RESERVED RESERVED RESERVED	H2SYNC GENERICC GPIO8 GPIO21_BB_EN			NA NA NA NA
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function (DEFAULT) 0 1 Audio for DisplayPort only 1 0 Audio for DisplayPort and HDMI if dongle is detected 1 1 Audio for both DisplayPort and HDMI		NA NA



GPIO 13,12,11 CONFIG[2:0] =>101 for PM25LV010

FLEX Computing

Project Name : H710DI1	Title : Capilano_STRAPS/ChipDiff	
Size :	Document Number : HPMH-40GAB6600-B130	Rev : B
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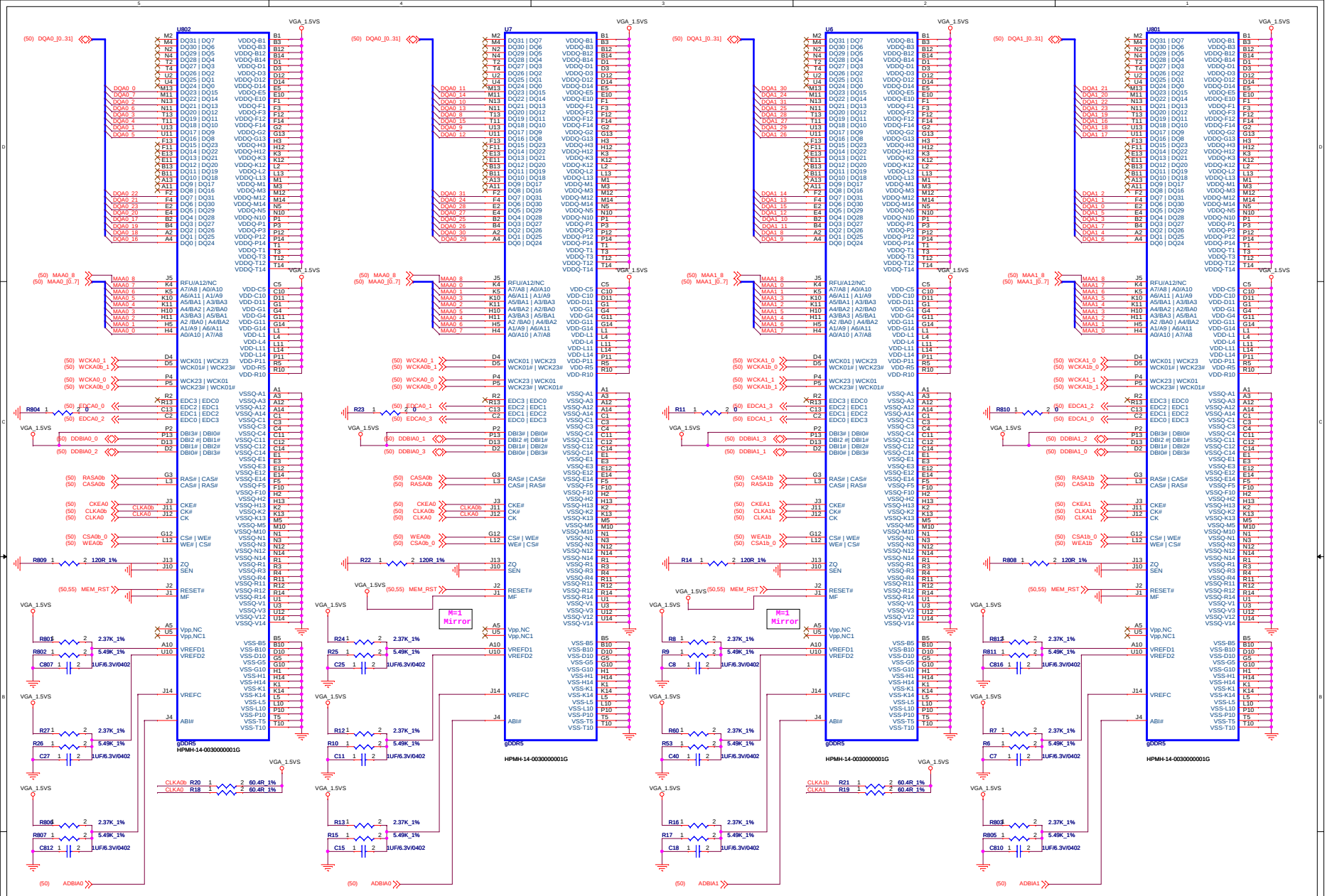

NA for Seymour

GDDR5 Memory Channel A X16 Mode

FLEXComputing		
Project Name : H710DI1	Title : Capilan_VRAM GDDR5 64MX16 A	
Size : B	Document Number : HPMH-40GAB6600-B130	Rev : B
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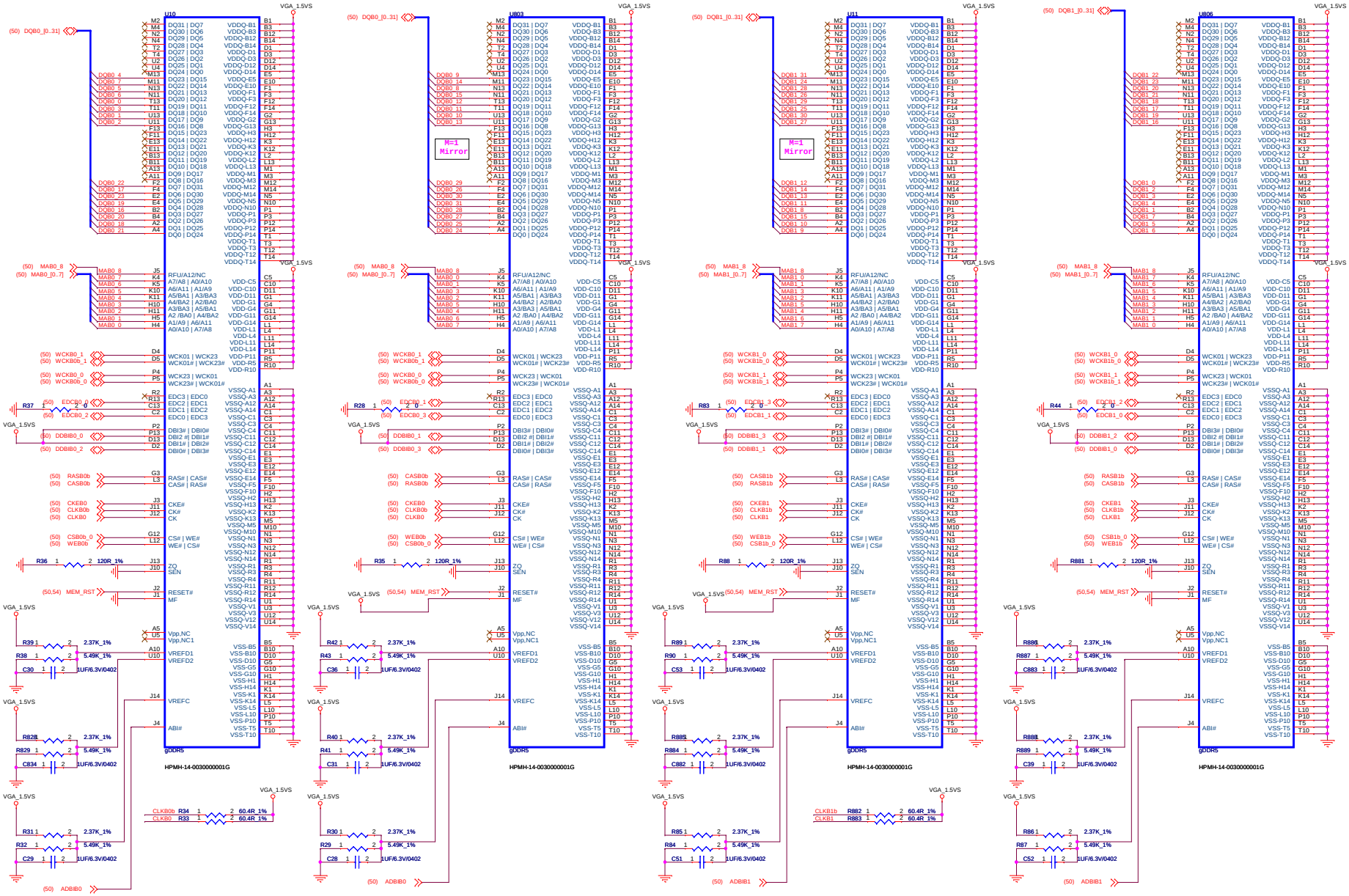
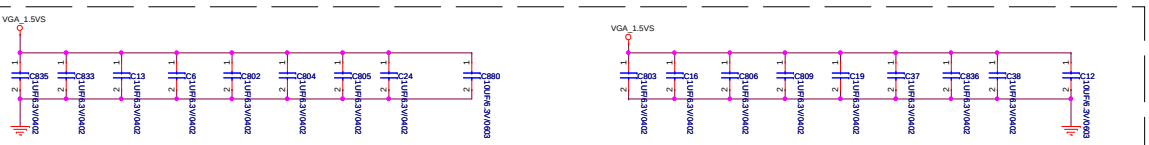


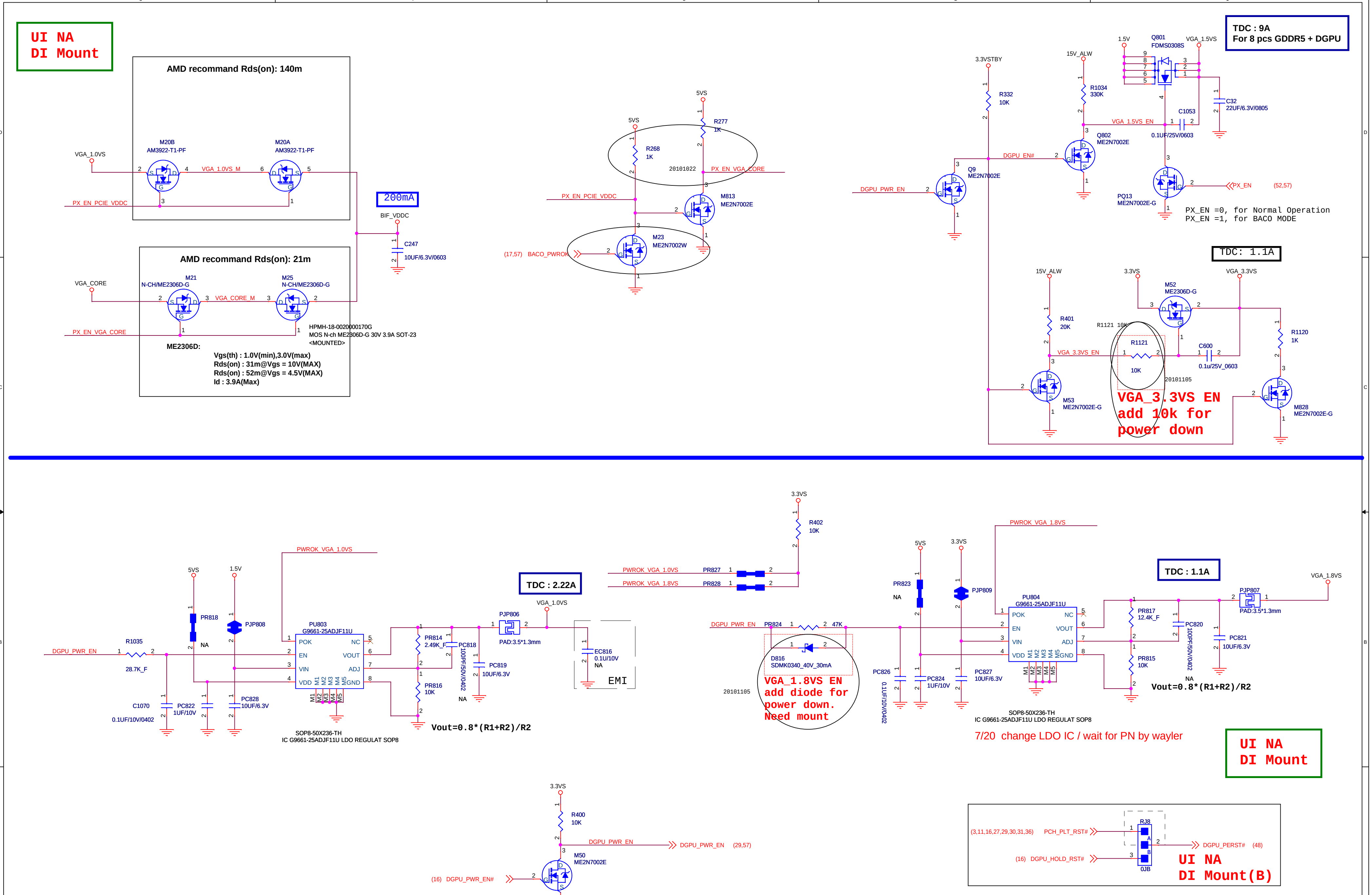
GDDR5 Memory Channel B X16 Mode



Decoupling caps for clamshell configuration:
1X 10uf per 2 clamshell DRAM
8 X 1uf per 2 clamshell DRAM

FLEX Computing

Project Name : H710DI1	Title : Capilan_VRAM GDDR5 64MX16 B
Size :	Document Number : HPMH-40GAB6600-B130 Rev : B
Date: Monday, November 08, 2010	Sheet : 55 of 63



L	H
DGPU ON	DGPU OFF

FLEX Computing

Project Name : H710DI1

Title : DGPU_RUN PWR, PWRGD, BACO

Size : B

Document Number : HPMH-40GAB6600-B130

Rev : B

Date: Monday, November 08, 2010

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VID4(PP2) (GPIO16)	VID3(PP1) (GPIO20)	VID2(PP0) (GPIO15)	VGA_CORE
0	0	1	1.05V
1	0	0	0.900V

VID							V_{DAC} (V)
6	5	4	3	2	1	0	
0	1	0	0	1	0	0	1.0500
0	1	1	0	0	0	0	0.9000

	15W	15W
TDC	15A	35A
OCP	22.5A	50A

深藍色框內爲15W NA

深藍色框內爲15W NA

深藍色框內爲15W NA

深藍色框內爲15W NA

深藍色框內爲15W NA

深藍色框內爲15W NA

15W 時需改值

15W 時MOUNTED

**TPS51728

5VS PU maybe leakage in BACO. Change to VGA_3.3VS

VGA_CORE EN change R and C for power down

PX_EN =0, for Normal Operation
PX_EN =1, for BACO MODE

OD, PU is at PCH/SB

TPS51217

PC17
35W==>HPMH-31-0020000064G 0.22u/25v_0603
15W==>HPMH-31-141047-950G 0.1uF/25V/0603

PL803
35W==>HPMH-32-800562-020G 0.56uH 25A PCMC104T-R56MN
15W==>HPMH-32-4000000181G 1uH 18A PCMC104T-1R0MN

PR6
35W==>HPMH-30-220021-990G 20K_0402_F
15W==>HPMH-30-154921-990G 54.9K_0402_F

PR13
35W==>HPMH-30-001006-990G 10_0402_J
15W==>HPMH-30-107521-990G 7.5K_0402_F

15W 時需改值

Seymour GDDR5 (15W)	
VID0	VGA_CORE
0	0.9
1	1.1

FLEX Computing

Project Name : H710DI1	Title : VGA_CORE(TPS51728)35W
Size : Custom	Document Number : HPMH-40GAB6600-B130
Rev : B	
Date: Monday, November 08, 2010	Sheet : 57 of 63

FID9 FIDUCIAL CAD-016 NC, NO CONNECT TO ANY.

FID802 FIDUCIAL CAD-016 NC, NO CONNECT TO ANY.

FID11 FIDUCIAL CAD-016 NC, NO CONNECT TO ANY.

FID804 FIDUCIAL CAD-016 NC, NO CONNECT TO ANY.

FID801 FIDUCIAL CAD-016 NC, NO CONNECT TO ANY.

FID10 FIDUCIAL CAD-016 NC, NO CONNECT TO ANY.

FID803 FIDUCIAL CAD-016 NC, NO CONNECT TO ANY.

FID7 FIDUCIAL CAD-016 NC, NO CONNECT TO ANY.

H26 PTH8_2.8 THR315B276_110 NA
H27 PTH8_2.8 THR315B276_110 NA
H25 PTH6.8_2.8 THR268_110 NA

CPU
H22 PTH7_4.7 THR276B189_150 NA
H23 PTH7_4.7 THR276B189_150 NA
H16 PTH7_4.7 THR276B189_150 NA
H17 PTH7_4.7 THR276B189_150 NA

H20 PTH6B7_2.8 THR236B276_110 NA
H12 PTH7_2.8 THR276B315_110 NA
H7 PTH7_2.8 THR276B315_110 NA AG
H8 PTH7_2.8 THR213B315_110 NA
H15 PTH7_2.8 THR276B315_110 NA

VGA
H18 PTH7_4.7 THR276B189_150 NA
H19 PTH7_4.7 THR276B189_150 NA
H13 PTH7_4.7 THR276B189_150 NA
H14 PTH7_4.7 THR276B189_150 NA

PCH
H11 PTH7_4.6 THR122B276_083
H10 PTH7_4.6 THR122B276_083

H9 PTH7_2.8 THR268B276_110 NA

H21 PTH7_2.8 NPTH106X087 NA
H24 PTH7_2.8 NPTH106X087 NA
H6 PTH7_2.8 NPTH087 NA

5VSTBY
放在gfx power 兩邊
C11241 2 0.1UF/10V/0402
C11251 2 0.1UF/10V/0402
C11281 2 0.1UF/10V/0402
C11271 2 0.1UF/10V/0402
1.05VS
C11311 2 0.1UF/10V/0402
C11301 2 0.1UF/10V/0402
C11451 2 0.1UF/10V/0402
for Intel Reserved

ME1 ME4 ME5 NA
ME2
20101103

5VS 5VSTBY
C820 1 2 NA 0.1UF/10V/0402
C46 1 2 NA 0.1UF/10V/0402
C1008 1 2 0.1UF/10V/0402
C506 1 2 0.1UF/10V/0402
C163 1 2 0.1UF/10V/0402

3.3VS CPU_CORE
C535 1 2 NA 0.1UF/10V/0402
C512 1 2 NA 0.1UF/10V/0402
C1139 1 2 0.1UF/10V/0402
C1140 1 2 0.1UF/10V/0402
C1141 1 2 0.1UF/10V/0402
C1142 1 2 0.1UF/10V/0402

1.5V
C533 1 2 0.1UF/10V/0402
C541 1 2 0.1UF/10V/0402
C539 1 2 0.1UF/10V/0402
C1143 1 2 0.1UF/10V/0402
C1144 1 2 0.1UF/10V/0402
CB853 1 2 0.1UF/10V/0402
20101102

5VSTBY 3.3VS
C496 1 2 NA 0.1UF/10V/0402
C518 1 2 NA 0.1UF/10V/0402
C181 1 2 NA 0.1UF/10V/0402
C126 1 2 NA 0.1UF/10V/0402
C84 1 2 0.1UF/10V/0402
C337 1 2 0.1UF/10V/0402
C1136 1 2 0.1UF/10V/0402
C1137 1 2 0.1UF/10V/0402
C1138 1 2 0.1UF/10V/0402
CB879 1 2 0.1UF/10V/0402
20101105
20100923

3.3VS VGA_1.5VS
C393 1 2 NA 0.1UF/10V/0402
C200 1 2 NA 0.1UF/10V/0402
C201 1 2 NA 0.1UF/10V/0402
C473 1 2 0.1UF/10V/0402
C215 1 2 NA 0.1UF/10V/0402
C236 1 2 0.1UF/10V/0402
CB852 1 2 0.1UF/10V/0402
20101102

3.3VS VGA_CORE
C390 1 2 NA 0.1UF/10V/0402

5VSTBY 1.05VS
C49 1 2 0.1UF/10V/0402

1.05VS 3.3VS
C164 1 2 NA 0.1UF/10V/0402
C323 1 2 NA 0.1UF/10V/0402
C526 1 2 0.1UF/10V/0402
C60 1 2 0.1UF/10V/0402
C1133 1 2 0.1UF/10V/0402
C1134 1 2 0.1UF/10V/0402
C1135 1 2 0.1UF/10V/0402
20100923

3.3VSTBY 3.3VS
C509 1 2 0.1UF/10V/0402
C532 1 2 0.1UF/10V/0402

3.3VS 1.05VS
C373 1 2 NA 0.1UF/10V/0402
C229 1 2 NA 0.1UF/10V/0402

3.3VS 5VSTBY
C499 1 2 NA 0.1UF/10V/0402

5VSTBY B+
CB49 1 2 0.1UF/25V
C1150 1 2 1UF/25V
CB4 2 1 1UF/25V
CB3 2 1 1UF/25V

B+ 3.3VS
CB90 1 2 0.1UF/25V
CB848 1 2 0.1UF/25V
CB122 1 2 0.1UF/25V
CB106 1 2 0.1UF/25V
CB5 1 2 0.1UF/25V
CB48 1 2 0.1UF/25V
CB878 1 2 0.1UF/25V
CB803 1 2 0.1UF/25V
CB847 1 2 0.1UF/25V
CB849 1 2 0.1UF/25V
CB850 1 2 0.1UF/25V
CB851 1 2 0.1UF/25V
20101102

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Project Name : H710DI1	Title : PAD_SCREW_ Moat Cap	
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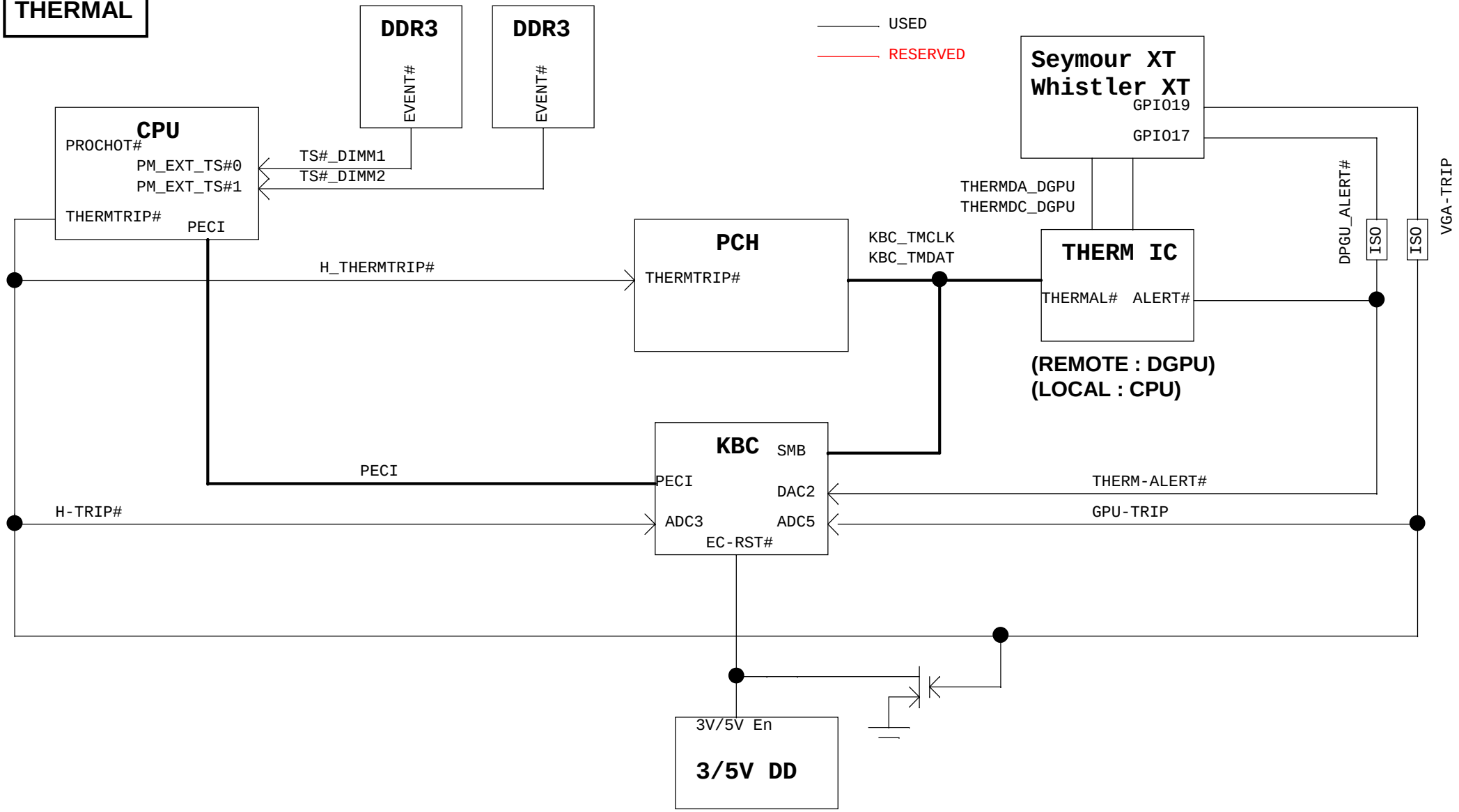
THERMAL



FLEX Computing		
Project Name : H710DI1	Title : Thermal Policy	
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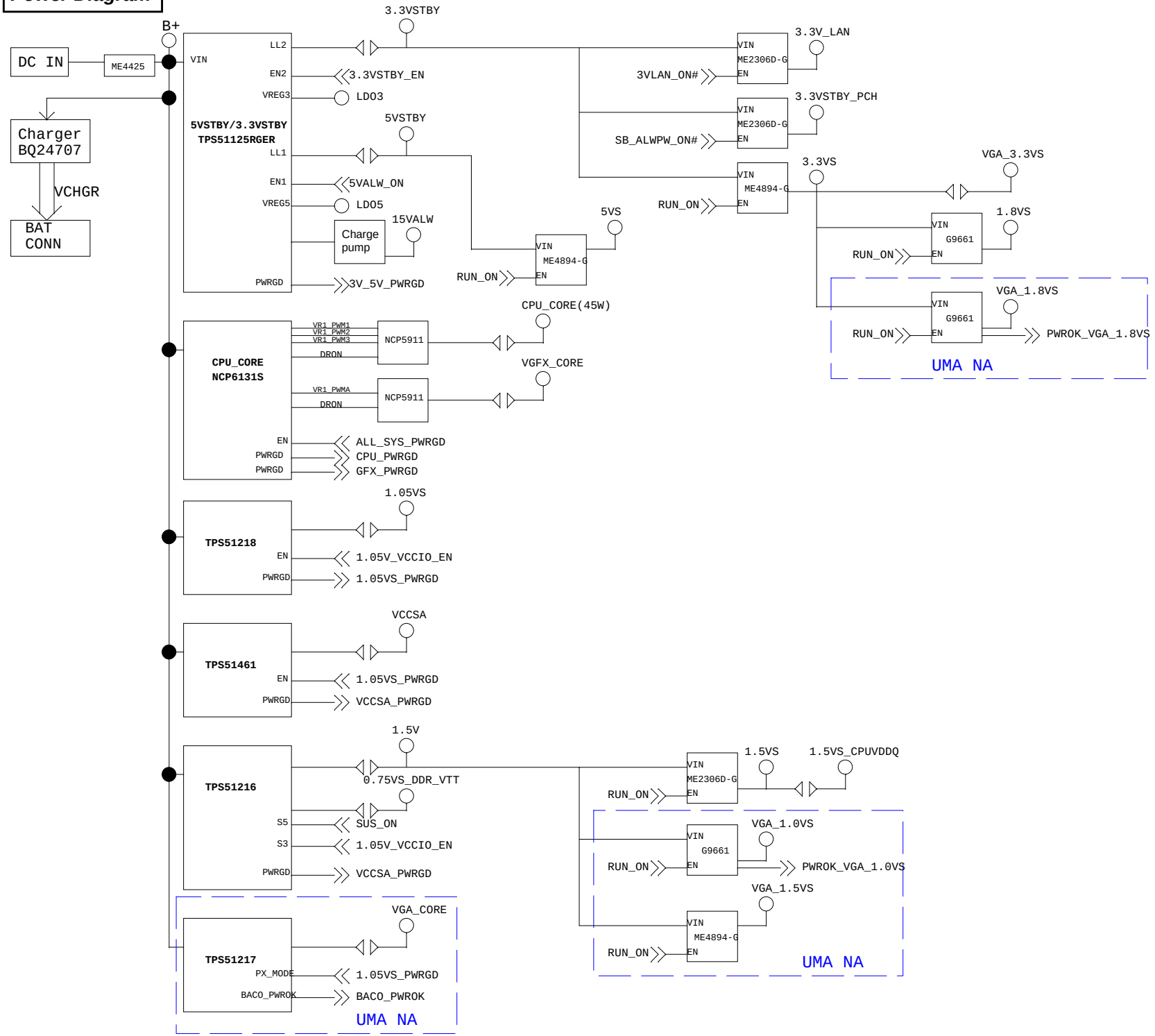
Power Diagram



FLEX Computing		
Project Name: H710DI1	Title: Power Diagram	
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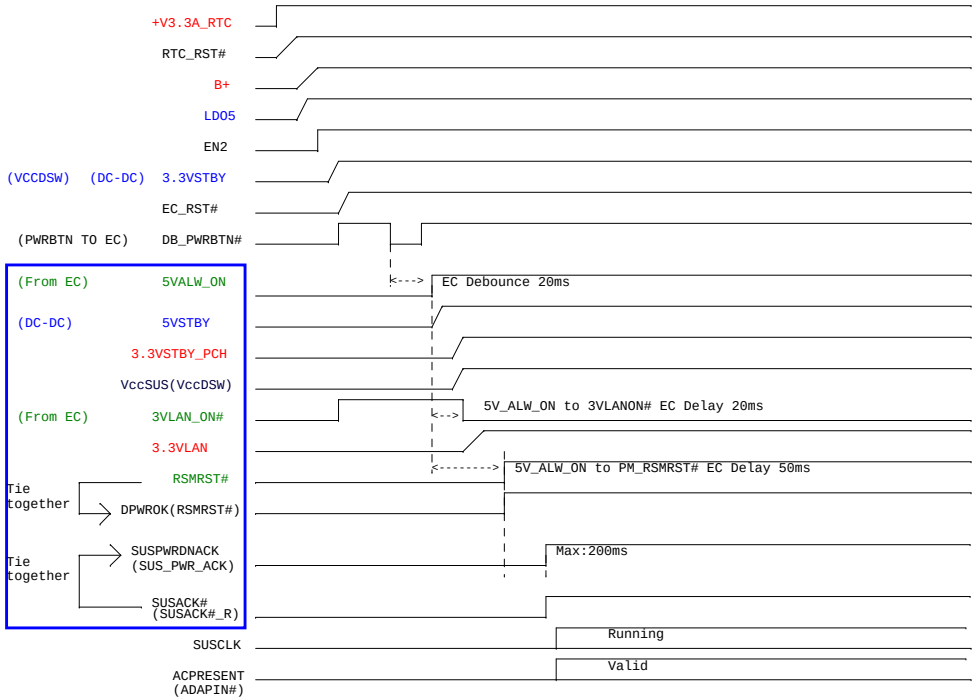
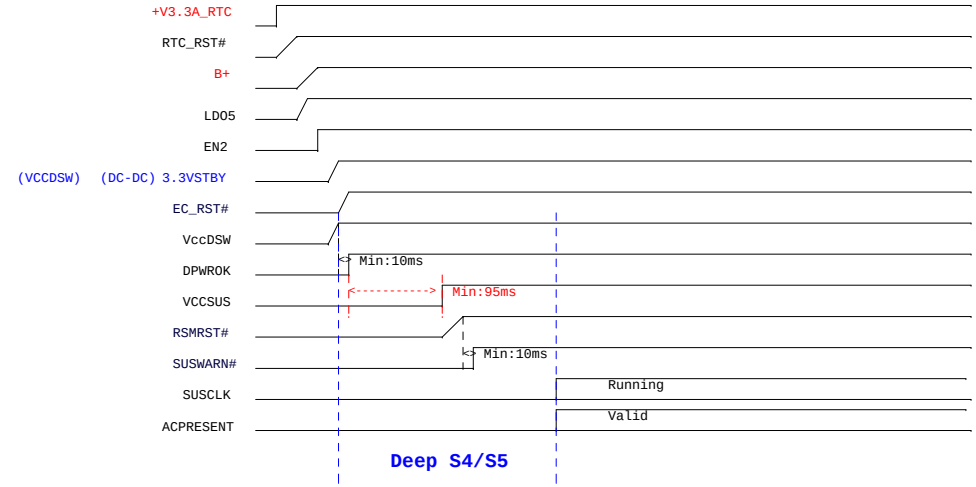
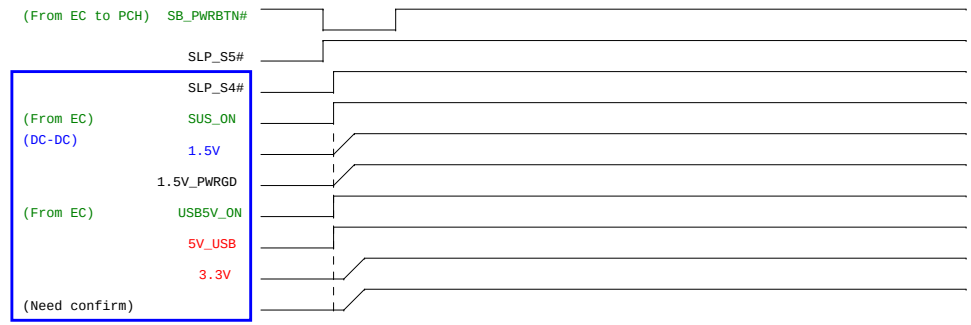
G3 to S0 (without Deep S4/S5)

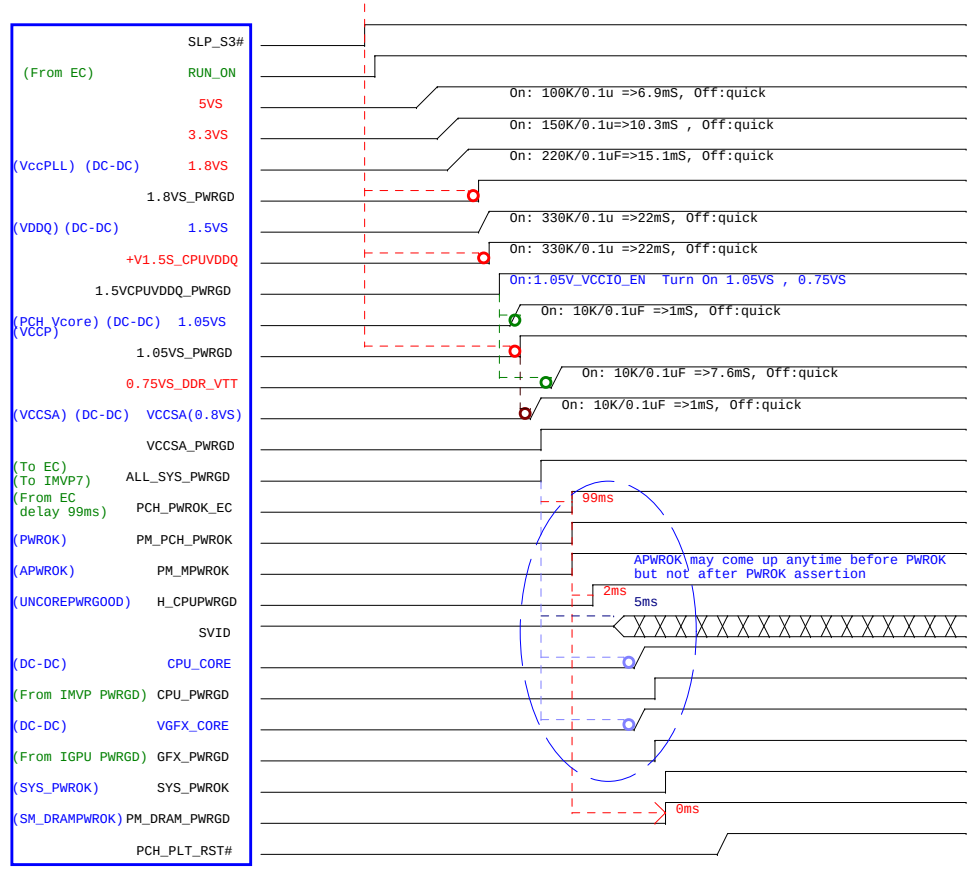


G3 to Sx (support Deep S4/S5) This Platform Without SUPPORT



S5 to S0





Blue: PWM

Green: EC

RED: MOSFET or Others

FLEX Computing			
Project Name : H710DI1		Title : POWER ON SEQUENCING	
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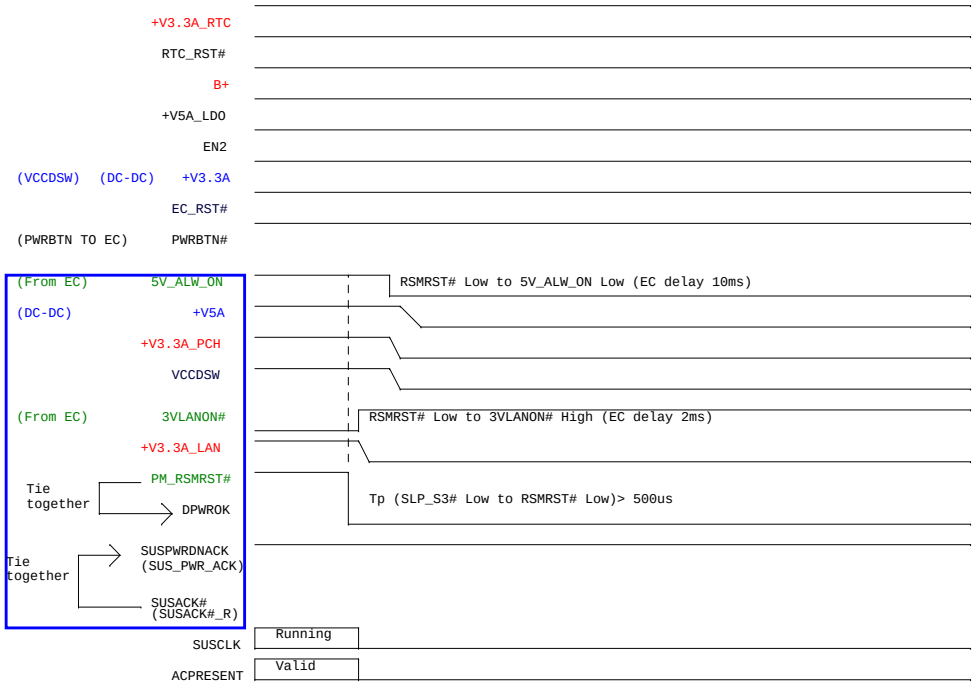
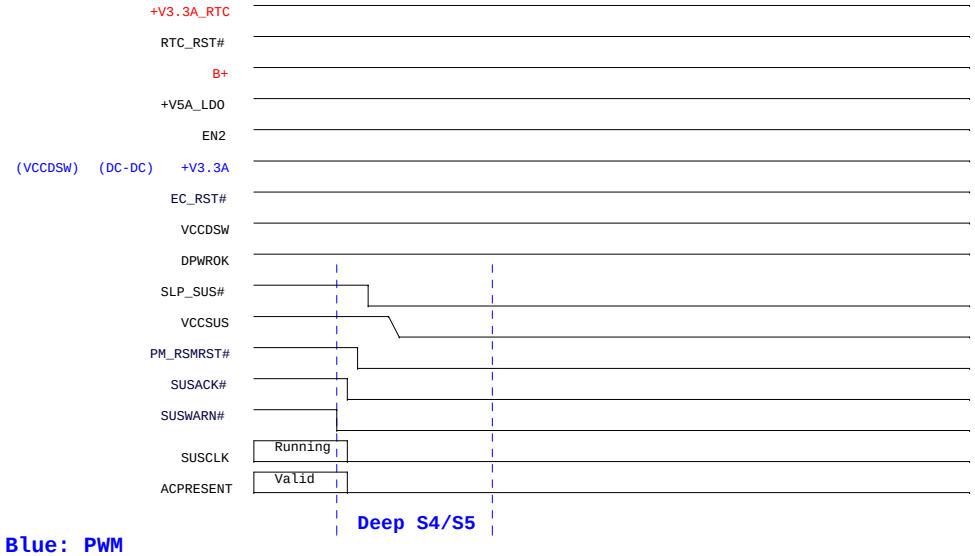
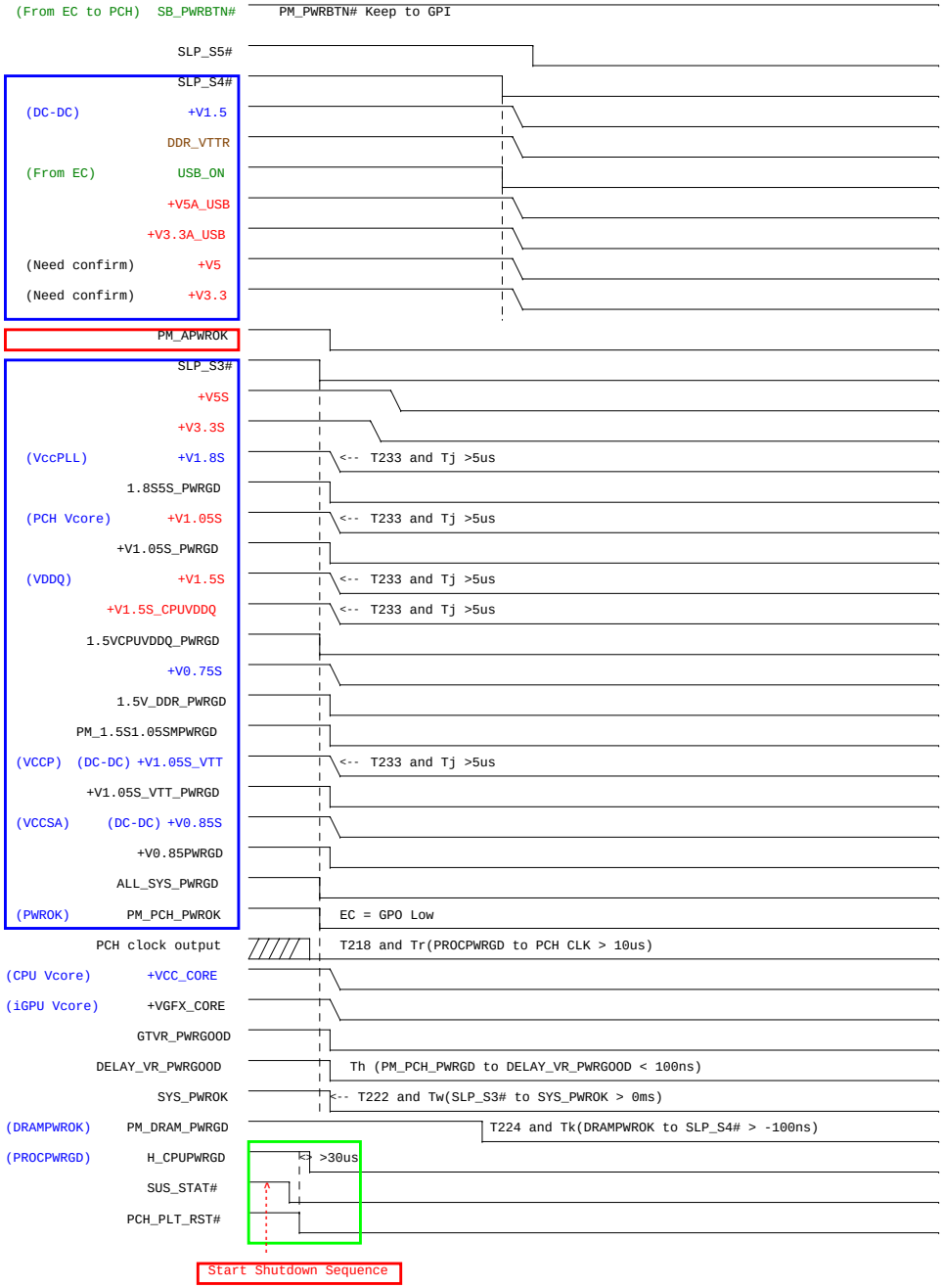
S0 to S5 (WoLAN Disable) (without Deep S4/S5)



S0 to S5 (support Deep S4/S5)



S0 to S4/S5



Blue: PWM

Green: EC

RED: MOSFET or Others

FLEX Computing			
Project Name: H710DI1		Title: POWER OFF SEQUENCING	
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MPHM-40GABE100-A1A0
K3 B 10K(MPHM-30-301036-990G) 010
K1804 B 10K(MPHM-30-301036-990G) 020
H104#11 MPHM-75110-000000S0 PWA NUT G AB610 020
PC99 MPHM-31-1F1007-900G 010
PC123 MPHM-31-163328-940G 010
PC124 MPHM-31-163328-940G 010
PR822 MPHM-30-178721-990G 020
PC805 MPHM-31-1F1007-900G 020
PR157, PR158, PR159, PR811 料號改爲MPHM-30-249991-990G
CB77 NA
CB78 NA
CN_KBL6 NA
M807 NA
M808 NA
R991 NA
R986 NA
C1006 NA
R1047 改爲MPHM-30-101546-990G RES CHIP 150KOHM J 0402
PR100 改爲MPHM-30-202241-990G RES CHIP 220Kohm F 0402
PC103 改爲 I:MPHM-31-1M1047-940G
CAP CERA CHIP 10V 100nF K X7R 0402
PR79改爲MPHM-30-202241-990G RES CHIP 220Kohm F 0402
PR148 改爲MPHM-30-301036-990G RES CHIP 10Kohm J 0402
PR839 改爲MPHM-30-301036-990G RES CHIP 10Kohm J 0402
C1099,C1091,C1092,C1093,C1087,C1086,R1065 NA
R1064,C540,C536,R1066,C1088 NA
Add MPHM-B2955807000001 HDMI COST FOR CASABLANCA AB610

20100830(base on A1A0 modify for SI)
change footprint CAP0402_BGA to CAP0402
change footprint RES0402_BGA to RES0402
change PN MPHM-18-00200001680 to MPHM-18-00200002020
change Q803 & Q8 frome MPHM-18-003904-900G to MPHM-18-00000000231G
M814 & PD9 NA
change FB81 footprit from POLYSW-SMDC035 to FUSE-3L4X1W8X1H
Connect PRDCHOT to IMVP7

20100831
Del R91
Change BT_DET# frome EC pin 73 to PCH PGIO6
Change BT_PWRON# frome EC pin 20 to PCH PGIO16
Add R1068,R1067,M822
R899 NA

20100901
Change U22 footprint SOIC8-50X286

20100906
change PR106 to 150K
modify new CN_KB6 footprint (CN-FPC-32P-1P0-2H)
modify new CN_CARD6 footprint CN-21N1CARD-11P-3H85)
modify CN_WOF6 footprint to CN-WTB-2P-1P25-2H03

20100907
change M13,M14,M18,M19,M16,M17,M22,M23
footprint TH0276B109_150
Modify CN_RTC801 footprint to CN-WTB-2P-1P25-4H9
Modify CN_WOF6 footprint to CN-WTB-2P-1P25-2H03
Modify CN_SPK7 to CN-WTB-4P-1P25-4H9
Modify R840/R841/R847/R848 2.49k change to 1.96k_F
(PN: MPHM-30-000000018361)(RES CHIP 1.96KOhm F 0402
Add R1069

20100910(A)
Del DPA34,RB51 NA
Modify USB 3.0 SMI connect to PCH
Page 35 modify Audio Woofer Schematics
Page 28 modify Thermal Schematics
20100910(B)
Del PD9
C868 change to 1uF/25V_0603 (PN: MPHM-31-0010000012G)
(CAP CERA 25V 1uF K X5R 0603)

20100911
ADD PC166-PC169 to 1500pF (PC166,PC167 NA)

20100913
modify C111 from 470uF to 330uF
Modify PR649,PR686 footprint to 0603 package
Add PR173(VRHOT# pull high)
PC878 change to 10nF
Delete CB858
Add FL1 (PJP004 open)
PR810 change to 2.2ohm.
Change PECI Pad36 to Pad820

20100915
Modify PS6 M20 Description to 140m
Modify FL1 Part number to PN
Modify CN_DUSB6 P18 from 5VSTBY to GND
and footprint from CN-FPC-18P-0P5-2H to CN-FPC-18P-1P0-2H
Modify LVDS CONN footprint CN-LVDS-40P-1H95 to CN-LVDS-40P-0P5-1H4
Modify CN_RTC801 footprint to CN-WTB-2P-1P25-4H9
Modify CN_WOF6 footprint CN-WTB-2P-1P25-2H03
Modify CN_SPK6 footprint CN-WTB-4P-1P25-4H9
Change VMEM_CSA#B0(Pad 36 to Pad 820)
Change PECI (Pad820 to Pad36)
Change PCH(U811)PN to MPHM-10-D010000113G
IC Cougar Point PCH 9XXL FCBGA989
modify U810 Pin40,Pin41,Pin43,Pin44
Add U808 Pin2,5,11,14 netname
Modify P36 USB3.0 from TI to NEC
Modify P37 USB3_1.1V to 1.05V_USB

20100916
modify Audio CN_SPK6 and CNSPK7 footprint again

20100917
modify CN_DUSB6 Footprint
Del PR165~PR172,Del PC170~173
Modify GDD Zero Power Schematics
NC_PCH_GPIO49 change to SATA_ODD_PRSNT#
SATA_ODD_PRSNT#(GPIO36) change to NC_PCH_GPI36
Del Pad29 R964 , Add R1110
Add C1119 for SER1MQ,C1120 for LPC_CLK
Modify PR677 to 26.1K ,PR144 to 80.6K
U19 Pin 73: 跑io改THERM_ALERT#(本來的pin78) ,
原本的 BT_DET# 移至 (Intel change to SB)
U19 Pin78: 跑回AC_OFF, 原本的THERM_ALERT#移到Pin73
Add PQ826 and PR879
Add R823 M824 for Touch Pad LED
Add JSR45,M825 for USB3.0 SMI
Update M.E. modification of screw holes (H20, H25)

20100923
modify PR160 to 4.7K(MPHM-30-247011-990G)
modify PR163 to 39K(MPHM-30-139021-990G)
modify PLB10 to 0.47uH (MPHM-32-400000027G)
PC113 change to MOUNTED
PR108 change to 1 ohm and mountted.(MPHM-30-200106-950G)
PC119 change to 470PF/50V and mounted (MPHM-31-1047J-940G)
PR851 change to MOUNTED.
Add PQ13,PQ29,C1130,C1131,PC77,CB84,CB842~CB846
Del PJP9,JS32,D8,M26,R301
CB68, C48 change from N.A to 33pF
CB317, EC818 change from N.A to mount (220PF)
CB66, CB61 change from N.A to mount (150pF)
增BACO_PWROK(GPIO2)改爲NC_PCH_GPI2
DGPU_PWROK (GPIO17) 改爲BACO_PWROK
NC_PCH_GPI50 (GPIO50) 改爲DGPU_HOLD_RST#
NC_PCH_GPI54 (GPIO54) 改爲DGPU_PWR_EN#
VGA_1.8VS, VGA_1.0VS, VGA_3.3VS,VGA_1.5VS,VGA_CORE 增enable改爲DGPU_PWR_EN
R879 ,R880 改爲L879,L880
EC819, EC811, EC812, EC813 change from N.A to 220pF
ED802, ED801, ED803, ED804 change from N.A to mount
(Flex P/N: MPHM-21-0200000012G, Footprint: CAP0603)
EC894, EC895, EC896, EC897 change from N.A to 220pF
PC878, PC871 change from 47pF to N.A
PR895, PR124, PR126, PR127 change from N.A to short pad
PR865, PR124, PR126, PR127 change from N.A to short pad
PC136, PC137, PC140, PC810 change from N.A to 1000pF
PR810, PR153, PR154, PR151 change from 0ohm to 2.2ohm
Add C1132 for KB_RST#
PR847 change from N.A to short pad
PC857 change from N.A to 1000pF
PR107 change from N.A to short pad
PC104 change from N.A to 1000pF
(C49, C580, C532, PC835, PC122, PC186, PC57, PC48, PC878, PC811, PC801, PC882, PC813 C256, C60, C84, C337, C473, C236, C533, C541, C539, C188, C586, C163 change from N.A to 0.1uF)
Add C1133-C1145
Add EM1~EM5
JS14/JS13/JS35/JS830 footprint change to RES0603-SHORT10
change C1037 to 0603 25V
Modify CN_DUSB6
change R1188 to 10K
Change C234,C235,C942,C944 to 0.1uF

↑ 10/19 REV.B100

change to Rev.C
1.modify CN_LVDS6 pin swap
2.Add R1116 for the LOGO
3.Modify PQ826 footprint
4.PR15 Pin 2 changes from 3.3VS to 5VS.
5.PR34 mounted and change to 90.9K (MPHM-30-00000001130G) for voltage slew.
6.PR8 changes NA.
7.Pin 1 of PR10 changes from 3.3VS to 5VS.
8.PR49 and PR52 change from 2.2 ohm to 0 ohm (MPHM-30-000006-950G)
9.PC17 and PC16 change from 1uF to 0.22uF (MPHM-31-002000004G)
10.PQ807 and PQ805 change from FDS6762 to NTMFS4928N (MPHM-18-002000024?6)
11.PQ806 and PQ801 change from FDM03085 to NTMFS4935N (MPHM-18-002000024G6)
12.PL803 and PL801 change from 0.45uH to 0.56uH (MPHM-32-000562-020G)
13.PR6 changes from 20K to 64.9K (MPHM-30-164921-990G) . (not 54.9K)

20100822
1.R277,R268 change from 10K to 1K for PX_EN_VGA_CORE rise time
2.swap LB17(1,4 pin對調;2,3 pin對調)
3.SW NA(swB for debug use)
Del CE6 , CE801,Add CE1 for USB3.0 cost

20100825
1.modify U25 Main source to MPHM-12-007408-620G

20101027
1.modify PCB PN to MPHM-41-AB620D-C00G
2.Add HDMI Label
3.Add Intel CPU PN table in P2
4.Add Intel PCH PN table in P12
5.Add R1117 100ohm for HP LOGO(eDP Conn)
Page 37
6.Update the net name of PU801 pin 3 as 1.5V_G9661.
7.Update the net name of PU801 pin 4 as 5V_G9661
Page 40
8.PR100 change to 0805 size (MPHM-30-291006-900G)
9.PC80 change to 0603 size (MPHM-31-001000012G)
Page 41
10.PR69 change to 34.8K_F (MPHM-30-234821-990G)
11.PR68 change to 22K_F(MPHM-30-222021-990G)
Page 43
12.PR127, PR126, PR124, PR805 change to 1 ohm 5% (MPHM-30-200106-950G)
Page 44
13.update switching frequency to 430KHz
14.update OCP to 15.54A
Page 45
15.update switching frequency to 700KHz
Page 46
16.update the value of PL812 to PCMC104T-1R0MN
17.update OCP to 19A
Page 57 (please replace whole page),
18.update VID table for 35WDGPU(x2) and 15WDGPU (x1)
19.PR7 change to 15K_F and to be NA (MPHM-30-000000007BG)
20.PR10 change to mounted.
21.PR9 change to NA.
22.Pin1 of PR30 change to 5VS.
23.PC9 change to NA.
24.Pin2 of PR45 change to GND and to be NA
25.PR23 change to 30K_F and to be NA (MPHM-30-130021-990G)
26.modify R1070 footprint 1206 to 0805
27.modify L13 PN and footprint to 0603
28.modify USB3.0 power 3.3V_USB and 3.3V_USB_VDDA

20101028
1.Add pad29 for BIOS test
2.LB17 SWAP
3.change M23 from ME2N7002E to ME2N7002W
and footprint from SOT-23A to UMT-23
4.change C111 PN to MPHM-31-6B337Y-130G
5.D805 pin 3 pn2 swap for layout trace

20101029
1.modify U822 footprint
2.modify Page1 Block
3.modify PR34 as 150K
RES CHIP 150Kohm F 0402 MPHM-30-115031-990G

20101030
1.modify PC90 to CB90
2.modify PC835 to CB848
3.modify PC122 to CB122
4.modify PC186 to CB186
5.modify PC57 to CB5
6.modify PC48 to CB48
7.modify PC878 to CB878
8.modify PC802 to CB803
9.modify PC813 to CB847
10.modify PC51 to CB49
11.modify PC801 to CB4
12.modify PC811 to CB3
13.modify RJ6 from B to A for PV PWA.Rev
14.Add R1808 and RJ809
15.Del R68 & R59

20101101
1.modify D805 Pin2 and Pin3
2.Del C1103,C1106,C1107
3.modify C1109 to 0.1uF/10V
4.PJP023 change footprint to JUMPER3P5-SHORT
5.Add two PC880,PC881 (68uF/25V) at B+
6.Delete PJP5

20101102
1.Add R1118 for GPU_TRIP#
2.RBS2 NA
3.PR70 change to 54.9K
4.R1052,R1050,R1051,C1081,Q803,M820 NA
5.CB67, CB62, CB57 change from 22pF to 33pF =>EMI
6.CB58, CB64, CB68 change from 22pF to 10pF =>EMI
7.Add ECB20,ECB21,ECB22,ECB23 =>EMI
(PWR_LED and GND,HDD_ACT_LED# and GND
HDD_PARK_LED# and GND)
8.CB854,CB833,CB832,CB831,CB830,CB825,CB824,
CB823,CB821 change from N.A to 100pF
9.C878 change from 10pF to 6.8pF
10.C879 change from 10pF to 4.7pF
11.Add ECB24 between CR-SD_3V3 and GND
12.EC801, EC13, EC17, EC11 change from N.A to 0.1uF
13.ECB10, ECB11, ECB13, ECB12 change from 220pF to N.A
14.ER801,ER802,ER803,ER804 change from
shout pad to Bead 220ohm (MPHM-32-20000001006G)
15.modify ER801,ER802,ER803,ER804 footprint
from shout pad to L0805
16.Add CB849,CB850,CB851,CB852,CB853
17.modify CN_PBTN6 from 6 pin to 8 pin
18.modify LID to PWRBTN BOARD
19.Add 0.1uF*2pcs to net VCHGR CB854,CB855
20.Add 0.1uF capacitor between CHG_LED# and GND
CB856
21.modify RJ9 to B

20101103
1.M825 from mounted to NA
2.PR801 form 261K to 39K ohm for power up before USB3_PONRST#
3.Add metal spring EK2
4.L801, EL8 change from Bead 120ohm to Resistor 300ohm
5.Add ED819 between net SENSE_A and GND
6.ED809, ED14 NA but change footprint and PN
(MPHM-21-0200000012G, Footprint: CAP0603)
7.ED13, ED11 change from N.A to mount,change footprint,PN
(MPHM-21-0200000012G, Footprint: CAP0603)
8.ADD ESD protection component between net SENSE_A and GND
(MPHM-21-0200000012G, Footprint: CAP0603)
9.Add R1119 for PX_EN
10.modify net PROCHOT_EC# to PROCHOT_EC
11.modify EC pin73 from THERM_ALERT# to DGPU_PWR_EN
12.Add JS43,JS44,JS45 between 24787ADN0 and GND
13.CB69, CB63, CB59 change from 22pF to 33pF
14.Add D197
15.Add M828 R1120 for VGA_3.3VS
16 net N22020819 change net name to DGPU_EN#

20101104A
1.Add PR883,PR884,PC882
2.modify PCB80,PC881 footprint
3.Del PC28
4.Add VGA_CORE TDC/OCP table

20101104B
1.CB52,CB53,CB65,CB66 just change
component dimensions to ED52,ED53,ED65,ED66
2.Change ED52,ED53,ED65,ED66 PN to
MPHM-21-0200000012G, Footprint: CAP0603
3.Delete CB42,CB43
4.ED805,ED806,ED807,ED808 change
PN MPHM-21-0200000012G, Footprint: CAP0603
5.ED801 pin2 change from GND to AGND

20101105A
1.Change ED52,ED53,ED65,ED66 PN to
MPHM-21-02000000096, Footprint: CAP0402
2.ED805,ED806,ED807,ED808 change
PN MPHM-21-0200000012G, Footprint: CAP402
3.ED801 pin2 change from AGND to GND
4.EDB10,ED15 change from GND to AGND
5.Add CB870 between 5VSTBY and GND
6.Add DB16.R1121,JS834,M829
7.PR30,PR802 change pin1 to VGA_3.3VS

20101105B
1.PR820 change pin1 to VGA_3.3VS

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Size: | Document Number: MPHM-40GAB600-B130 | Rev: A
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